PREGLED VARIANT V SESTAVNICI

Var.	Ident variante	Naziv
01	24469044	ENOTA KRMILNA BP-01
		disk kontroler

Var.	Ident variante	Naziv

PREGLED IZDAJ IN SPREMEMB V SESTAVNICI

Izd.	Obvestilo	Datum obvestila	Št. sp.	Opis spremembe	Velja za varianto	Datum izdaje	Referent	Avtor izdaje	Podpis avtorja
01	12-079	86.12.09		NOVA SESTAVNICA	A / / / / /	9.12.86	03	KNEŽO F.	

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NASLOVNI LIST SESTAVNICE

ENOTA KRMILNA BP-01

Obvest. – Nalog	Datum izpisa	Izdaja	Ident sestavnice	Dekada	List
12-079	9.12.86	03	24469044	01	

V SESTAVNICI
A – aktiven (brez datuma)
– aktiven (do datuma)
N – neaktiven (brez datuma)
– neaktiven (do datuma)

A – embalaža
B – fantom, fiktivni del
C – surovec, odtisek, odlivek
D – kupljeni del (brez strukture)
E – lastni del (s strukturo)
G – usluge
I – drobni inventar
L – kabli, povezave, žice (odrezane na dolžino)
M – material, ki ga kupujemo
P – pomožni material, pribor
R – vzorci za razvoj
S – lastni sestav, ki se skladišči (sestavnica)
T – orodje
U – dokumentacija, literatura
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7 – kupljenec s klringa – ni naš razvoj
8 – kupljenec s konvertibilnega področja – ni naš razvoj
9 – kupljenec domači – ni naš razvoj
0 – prosto

EM – ENOTA MERE
1 – kos
2 – kg (kilogram)
3 – l (liter)
4 – m (meter)
5 – m² (kvadratni meter)
6 – m³ (kubični meter)
7 – g (gram)
8 – ml (mililiter)
9 – par (po dva kosa)
0 – garnitura

BF – BAZNI FAKTOR
0 – za 1 = 10⁰ kosov sestav.
1 – za 10 = 10¹ kosov sestav.
2 – za 100 = 10² kosov sestav.
3 – za 1000 = 10³ kosov sestav.
4 – za 10000 = 10⁴ kosov sestav.
5 – za 100000 = 10⁵ kosov sestav.
6 – za 1000000 = 10⁶ kosov sestav.

Poz.	Ident	Naziv	Napotilo	S	K	P	I	EM	BF	Količina za vnos A	Velja do
01A	24469044	ENOTA KRMILNA BP-01		A	S		2	1	0	*	
001	18908044	IC 74F00 TTL DIP P		A	M		8	1	0	3	
002	18910044	IC 74F04 TTL DIP P		A	M		8	1	0	3	
003	18911044	IC 74F09 TTL DIP P		A	M		8	1	0	3	
004	18912044	IC 74F10 TTL DIP P		A	M		8	1	0	2	
005	18920044	IC 74F138 TTL DIP P		A	M		8	1	0	2	
006	18923044	IC 74F133 TTL DIP P		A	M		8	1	0	3	
007	18924044	IC 74F157 TTL DIP P		A	M		8	1	0	1	
008	19345044	IC 74F161 TTL DIP P		A	M		8	1	0	3	
009	20969044	IC 74F175		A	M		8	1	0	1	
010	18929044	IC 74F219 TTL DIP P		A	M		8	1	0	4	
011	18930044	IC 74F240 TTL DIP P		A	M		8	1	0	1	
012	18931044	IC 74F244 TTL DIP P		A	M		8	1	0	5	
013	18932044	IC 74F245 TTL DIP P		A	M		8	1	0	2	
014	18933044	IC 74F251 TTL DIP P		A	M		8	1	0	3	
015	18937044	IC 74F299 TTL DIP P		A	M		8	1	0	5	
016	18941044	IC 74F373 TTL DIP P		A	M		8	1	0	3	
017	18942044	IC 74F374 TTL DIP P		A	M		8	1	0	10	
018	19800044	IC 74F521 TTL DIP P		A	M		8	1	0	1	
019	18917044	IC 74F74 TTL DIP P		A	M		8	1	0	5	
020	19946044	IC 74F86 TTL DIP P		A	M		8	1	0	2	
021	10164044	IC 74LS259 TTL DIP P	TP-K,09,114	A	M		8	1	0	1	
022	11505044	IC 74LS273 TTL DIP P	TP-K,09,114	A	M		8	1	0	2	
023	14927044	IC 74S05 TTL DIP P	TP-K,09,114	A	M		8	1	0	1	
024	18903044	IC 74S273 TTL DIP P		A	M		8	1	0	1	
025	14933044	IC 74S31 TTL DIP P	TP-K,09,114	A	M		8	1	0	1	
026	14694044	IC 75452 LIN DIP P		A	M		8	1	0	1	
027	10148044	IC 8640 LIN DIP P		A	M		8	1	0	1	
028	10150044	IC 8641 LIN DIP P		A	M		8	1	0	1	
029	10435044	IC 8837 LIN DIP P		A	M		8	1	0	1	

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SESTAVNICA

ENOTA KRMILNA BP-01

Avtor izdaje	Obvest. – Nalog	Datum izpisa	Izdaja	Ident sestavnice	Dekada	List
KNEGO P.	12-079	9.12.86	01	24469044	01*	1

A – aktiven (brez datuma)
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R – vzorci za razvoj
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T – tehnološki sestav, ki se ne skladišči
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1 – normativ
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Poz.	Ident	Naziv	Napotilo	S	K	P	I	EM	BF	Količina za vnos						Velja do
										A						
01A	24469044	ENOTA KRMILNA BP-01		A	S		2	1	0	*						
030	32668044	IC 96101 LIN DIP P		A	M		8	1	0	2						
031	18927044	IC 74F182 TTL DIP P		A	M		8	1	0	1						
032	21638044	IC AM2901CPC		A	M		8	1	0	4						
033	19937044	IC AM2908PC		A	M		8	1	0	8						
034	21576044	IC AM2911APC		A	M		8	1	0	3						
035	19938044	IC AM2922PC		A	M		8	1	0	1						
036	18803044	IC AM2925 DC		A	M		8	1	0	1						
037	18804044	IC AM2930 DC		A	M		8	1	0	2						
038	19901044	IC LM393		A	M		8	1	0	1						
039	21306044	IC MC3450P		A	M		8	1	0	7						
040	11893044	IC 3453P		A	M		8	1	0	7						
041	19933044	IC MK4801AN-55		A	M		8	1	0	2						
042	21567044	IC PAL 12L10CN TTL DIP P		A	M		8	1	0	1						
043	19620044	IC PAL 14L4ACN TTL DIP P		A	M		8	1	0	1						
044	19621044	IC PAL 16L2ACN TTL DIP P		A	M		8	1	0	1						
045	18958044	IC PAL 16R8ADJ TTL DIP K		A	M		8	1	0	1						
046	19791044	IC PAL 16L8CN TTL DIP P		A	M		8	1	0	4						
047	11306044	TRANZISTOR BC182		A	M		9	1	0	1						
048	13647044	TRANZISTOR BC212		A	M		9	1	0	2						
049	17164044	TRANZISTOR BFJ49		A	M		9	1	0	1						
050	13422044	DIODA BYF405	TP-K,06,145	A	M		9	1	0	1						
051	14113044	DIODA BA313	TP-K,06,106	A	M		9	1	0	2						
052	22917044	DIODA SVETLEČA SSO-0405		A	M		8	1	0	3						
053	32655044	JEDRO FERITNO FT22B 13/0805-03		A	M		9	1	0	1						
054	22913044	VTIČ PTIV ZAPRT OZEK*10U		A	M		8	1	0	1						
055	22914044	VTIČ PTIV ZAPRT OZEK*26		A	M		8	1	0	4						
056	22916044	VTIČ PTIV ZAPRT OZEK*60		A	M		8	1	0	1						
057	14719044	VTIČNICA MIN 65474-001		A	M		8	1	0	3						
058	14008044	UPOR PL-D AS 08*10K J	TP-K,03,126	A	M		9	1	0	1						

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SESTAVNICA

ENOTA KRMILNA BP-01

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Poz.	Ident	Naziv	Napotilo	S	K	P	I	EM	BF	Količina za vnos						Velja do
										A						
010	24469044	ENOTA KRMILNA BP-01		A	S		2	1	0	*						
059	22911044	UPOR SC 09-8*56R J		A	M		8	1	0	7						
060	22910044	UPOR SC 09-8*82R J		A	M		8	1	0	5						
061	20045044	UPOR PL-D AS 08*470R J	TP-K,03,126	A	M		9	1	0	7						
062	32738044	UPOR MPL MLT-0,125*1K8 J		A	M		9	1	0	2						
063	15605044	UPOR MPL MLT-0,125*180R J		A	M		9	1	0	4						
064	15608044	UPOR MPL MLT-0,125*390R J		A	M		9	1	0	2						
065	16531044	UPOR MPL MLT-0,125*470R J		A	M		9	1	0	20						
066	15628044	UPOR MPL MLT-0,125*100K J		A	M		9	1	0	1						
067	15620044	UPOR MPL MLT-0,125*10K J		A	M		9	1	0	4						
068	15611044	UPOR MPL MLT-0,125*1K J		A	M		9	1	0	4						
069	16533044	UPOR MPL MLT-0,125*1K2 J		A	M		9	1	0	2						
070	21169044	UPOR PL 02006*1M5		A	M		9	1	0	1						
071	13957044	UPOR PL 02006*56K J	TP-K,03,100	A	M		9	1	0	1						
072	32741044	UPOR MPL MLT-0,125*47R J		A	M		9	1	0	2						
073	32742044	UPOR MPL MLT-0,125*8K2 J		A	M		9	1	0	1						
074	14092044	KONDENZ TANTAL*22MY 16V	TP-K,02,101	A	M		8	1	0	1						
075	22912044	KRISTAL*27,125 MHZ		A	M		9	1	0	1						
076	13923044	UPOR PL 02006*120R J	TP-K,03,100	A	M		9	1	0	1						
077	18973044	KONDENZ KER*3N3 50V		A	M		9	1	0	1						
078	16665044	KONDENZ KER*470P 63V		A	M		9	1	0	1						
079	10542044	KONDENZ KER*270P 500V	TP-K,02,104	A	M		9	1	0	1						
080	14036044	KONDENZ KER*47N 32V	TP-K,02,109	A	M		9	1	0	2						
081	10079044	KONDENZ AL EL*100MY 25V	TP-K,02,105	A	M		9	1	0	2						
082	20255044	KONDENZ AL EL*47MY 16V	TP-K,02,107	A	M		9	1	0	1						
083	13913044	UPOR PL 02006*10R J	TP-K,03,100	A	M		9	1	0	1						
084	20408044	UPOR PL 02006*3K J		A	M		9	1	0	1						
085	32682044	DRŽALO PTIV 12-DESNO		A	E		6	1	0	1						
086	32680044	DRŽALO PTIV 12-LEVO		A	E		6	1	0	1						
087	22918044	IC 6389-2 PROG		A	Q		1	1	0	18						

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SESTAVNICA

ENOTA KRMILNA BP-01

Avtor izdaje	Obvest. – Nalog	Datum izpisa	Izdaja	Ident sestavnice	Dekada	List
KNEGO P.	12-079	9.12.86	01	24469044	01*	3

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Poz.	Ident	Naziv	Napotilo	S	K	P	I	EM	BF	Količina za vnos						Velja do
										A						
014	24469044	ENOTA KRMILNA BP-01		A	S		2	1	0	*						
088	14043044	KONDENZ KER*220N 50V	TP-K,02,115	A	M		9	1	0	30						
089	06251091	NOVICA B 3X0,3X12 ME	IS-F,07,15	A	M		9	1	0	4						
090	14155044	PODNOŽJE DIP SPAJK*18	TP-K,12,103	A	M		9	1	0	18						
091	14179044	PODNOŽJE DIP SPAJK*20	TP-K,12,103	A	M		9	1	0	7						
092	14161044	PODNOŽJE DIP SPAJK*24	TP-K,12,103	A	M		9	1	0	1						
093	22945044	PLOŠČA TIV-UNIBUS DISK KONTROLER		A	E		4	1	0	1						
094	14156044	DISTANČNIK MONT TO3/8	TP-K,12,107	A	M		9	1	0	1						

Iskra Delta

SESTAVNICA

ENOTA KRMILNA BP-01

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KNEGO P.	12-079	9.12.86	01	24469044	01*	4

asm A2-2803

BP-01 INTELLIGENT DISK CONTROLLER

DEVELOPMENT DOCUMENTATION

TABLE OF CONTENTS

1.2.2 General Description

The BP-01 controller consists of a six-layer printed circuit board which may be installed in any hex-wide UNIBUS SPC slot.

The controller supports any drive with a SMD compatible interface. Sector size is 512 bytes. Each sector has an ID block with the address (cylinder, head, sector) of the sector, a bad-sector flag and an ID-block ECC. The ID is written when the pack is initially formatted. In ordinary use (under an operating system, for example), the ID-block is read to verify correct posittioning before reading or writing a sector.

All signals required to perform direct memory access (DMA) operations with the host are provided by the controller. Preselectable solderless jumpers permit the controller to be assigned an I/O address in the host system.

1.2.3 Standard Features

The BP-01 controller includes the following standard features :

* The controller supports four drives ; they may be any combination of capacities, number of tracks and track formats (number of sectors per track). Special GDP function (Get Drive Parameters) allows the controller to find out parameters and to proceeds them to the system.(only for formatted drives).
* Single hex-wide DEC compatible PCB.
* Error Correction Code (ECC) provides up to 11 bit burst error correction on each sectors' data field.
* ECC doubleword on each sectors' header field
* Up to 768 byte (3 Sectors) data buffering to eliminate "Data Late" errors.
* Overlapped seek capability.
* UNIBUS throttle control

* Capability of attachment of removable media, fixed Winchester, or combination fixed/removable media SMD compatible disk drives.

* Automatic self-test microdiagnostics.

* Multiple sector data transfer up to 64k words per read /write operation.

1.2.4 Specifications

Specifications of the BP-01 controller are summarized below :

1.2.4.1 Functional Characteristics -

Disk Drive Interface	SMD
Drive Ports	4
Disk Interface Connection	
Control	Daisy Chain
Data	Radial
Base Register Address	
Standard	774000(8)
Alternative	774040(8)
Bus Address Range	0 - 128 K word
Vector Address	loadable (default 174(8))
Priority Level	BR5 standard
DMA Burst Control	1 to 256 words UB-throttle controlled
Sector Size	256 words (512 bytes)

Sectors/Track	any - no special selection required, up to 256.
Tracks/Cylinder	any - no special selection required, up to 127.
Cylinders/Drive	any - no special selection required, up to 1024.
Data Buffering	up to 3 sectors
Seek Operation Control	Explicit, implied and overlapped seek.
Data Field Integrity	ECC - 11 bit burst error detection and correction ; 32 bit ECC polinomial.
Header Field Integrity	32 bit ECC, auto position verification (Cylinder,Head, and Sector comparison)

1.2.4.2 Performance Characteristics -

Error Correction Time	Less than 6 mS in local buffer
Max Data transfer Rate :	
Disk	2.0 Mbytes/Sec
UNIBUS	2.4 Mbytes/Sec

1.2.4.3 Physical Characteristics -

PCB Size	Single hex wide 8.5"x15.0",6 layer PCB.
Cable Connections	One 60-pin flat cable connector and four 26-pin flat cable connector mounted at the edge of PCB.

1.2.4.4 Power Requirements -

+5 V dc, +5% or -5% at 7,5 amps
-15 V dc, +5% or -5% at 0.2 amps

1.2.4.5 UNIBUS Loading - BP-01 controller presents one unit load.

CHAPTER 2

HARDWARE DESCRIPTION

2.1 HARDWARE DESCRIPTION

The major logic sections and buses of the BP-01 are described briefly below. Figure 2-1 presents a functional block diagram of the BP-01. On the Figure 2-2 is presented micro word definition.

Fig.2 CONTROLLER MICROWORD ORGANIZATION

71 70 69	68 67 66	65 64 63	62 61 60 59	58 57 56 55	54	53	52
PROC DST	PROC FNC	PROC SRC	PROC B-FIELD	PROC A-FIELD	PR OE	PL OE	PB OB

51 50 49	48	47	46	45 44 43	42 41 40	39	38 37 36	35 34 33	32
V-BUS DST	W DT	C IN	D MA	BUS SRC	BUS DST	U MD	MUX SEL	ADC SEL	P OL

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11	10 9 8 7 6 5 4 3 2 1 0
"DATA" PIPELINE LITERAL FIELD	SEQUENCER INSTRUCTION	SEQUENCER LITERAL FIELD

2.1.1 Microprocessor

The main part of the controller is a bit slice designed Microprocessor using four AM 2901C ICs. Four static RAMs (16 4bit Words each are used to expand the microprocessors' register space (REG SPACE) to 32 16-bit working registers. Additional RAMs are referred to as P-registers, and they enable significant improvements in performance to be achieved.

P-registers are addressed from the micro-word through the "B" address field. Read/Write operations on P-registers are controlled by particular bit combinations in micro-word.

The Microprocessor gets data to D-inputs from the Pipeline register, P-register or from the D-bus, which is the controller PCB major data path (see Fig. 2-1). Microprocessors' data outputs are the only data sources for Y-bus. Y-bus destination are P-registers and various address pointers. Data can be transferred from Y-bus to the D-bus.

The sequencer for the Microprocessor consists of three AM 2911 ICs. The 2911 Sequencer provides the capability for addressing the control store from its program counter, "SI-bits" literal field, internal P-register or internal four-level Stack-file. The Sequencer performs jumps, conditional jumps, subroutine jumps and subroutine returns. Up to 32 individual jump conditions can be tested. As a special feature the Sequencer tests the Microprocessors' ALU status flags (CARRy, MINUS, ZERO) either from the previous or current micro-instruction. When status flags of the current microinstruction are tested, the next address generation is based on the results of the arithmetic operation and microprogram memory is accessed accordingly. The extended microcycle approach enables the standard microinstruction period to be shorter by 50%. Furthermore, microprogram space is saved by eliminating the need for additional memory access instructions. The microprogram space made available in this manner is used to implement functions that are not usually found in such controllers.

Microprogram execution could be interrupted if disk or Unibus microinterrupts occurred. A Unibus interrupt can be masked for a period of time when the Microprocessor is performing a time-critical function, while the disk interrupt cannot be masked. Disk interrupts occur during disk read or write operations whenever the R/W shift register is full or empty. The

Interrupt Control Logic provides an interrupt vector determined by the operation requested from the Unibus or disk drive. During the interrupt execution the 2911 outputs are disabled (CARRY IN in the Sequencer is held "0"), the ALU status flags are saved and the next address generation continues the "normal" microprogram-flow. There is only one "nonmaskable" interrupt input, handling the Power-up init, Unibus init and the WDT (Watch Dog Timer). If such an interrupt occurs, the microprogram sequencer starts an execution of the microprogram from the address zero.

2.1.2 UNIBUS Interface

The UNIBUS interface is controlled by the Microprocessor. The firmware transmits and receives data and addresses via Am2908 bus transceivers-registers. The UNIBUS arbitration and handshake logic is realized with the two 16L8 PALs. The UNIBUS CSR-s contained in 1Kx16 buffer RAM are directly accessible through the UB-Microinterrupt sequence.

2.1.3 Disk Interface

The Microprocessor loads information which is to be transferred to SMD A-cable, into two 74LS273 8-bit registers. All SMD bus DRIVERS and RECEIVERS are MC3453 and MC3450 respectively. Microprocessor controls selection of the logical disk drive, interrupt status from the drive, cylinder/ head selection, and selects one of four "B" cable ports for data transfer.

The serializer/deserializer (S/D) consists of two 74F299 eight bit shift registers to convert data from parallel to serial during Writes and from serial to parallel during Reads. Parallel data is transferred 16 bits at a time from the BUFFER comprised of two MK4801 RAMs through the two Am2950 multifunctional registers to S/D during Write operations on the D-BUS. During Read operations, data is transferred from the S/D shift registers 16 bits at a time through 2950s into BUFFER.

READ/WRITE logic, consisting of 16R8 PAL, 74F161 WORD-counters, and a 74F521 SYNC byte comparator, once enabled, performs a R/W functions described above automatically, transparent to the microprogram-flow, using a DISK-Microinterrupt sequence. All needed is, to prepare one of the three possible SECTOR-buffers in BUFFER RAM, and start the function. A 74F521 SYNC byte comparator is used to compare the SYNC byte read from

the disk against a pre-defined, hardwired constant (HEX 0019). This comparison is enabled when searching for SYNC during Reads or non-format Writes. Before start of the Write operations, a SYNC byte must be loaded into 2950 register.

Each logical sectors header and data field has four bytes of ECC code appended. The ECC polinomial is implemented using three 74F299, one 74S273, and five 74F86 EX-OR gates forming the feedback terms. The ECC polinomial divides the data field as it is written, and the 32 bit ECC is then appended to the data field. When the ECC is being written, it is shifted out without any feedback and acts as 32 bit shift register.

When a sectors header or data field is read, the ECC hardware again divides it by the fixed polinomial. The ECC registers are tested at the end of the ECC field, and if found to be non-zero, the data is in error. The ECC correction routine is entered to determine the bit(s) in error and location within the sector. The data is corrected depending of program control.

2.1.4 Disk Format

Sector consist of Header, Header ECC, Data and Data ECC and Gap Fields.

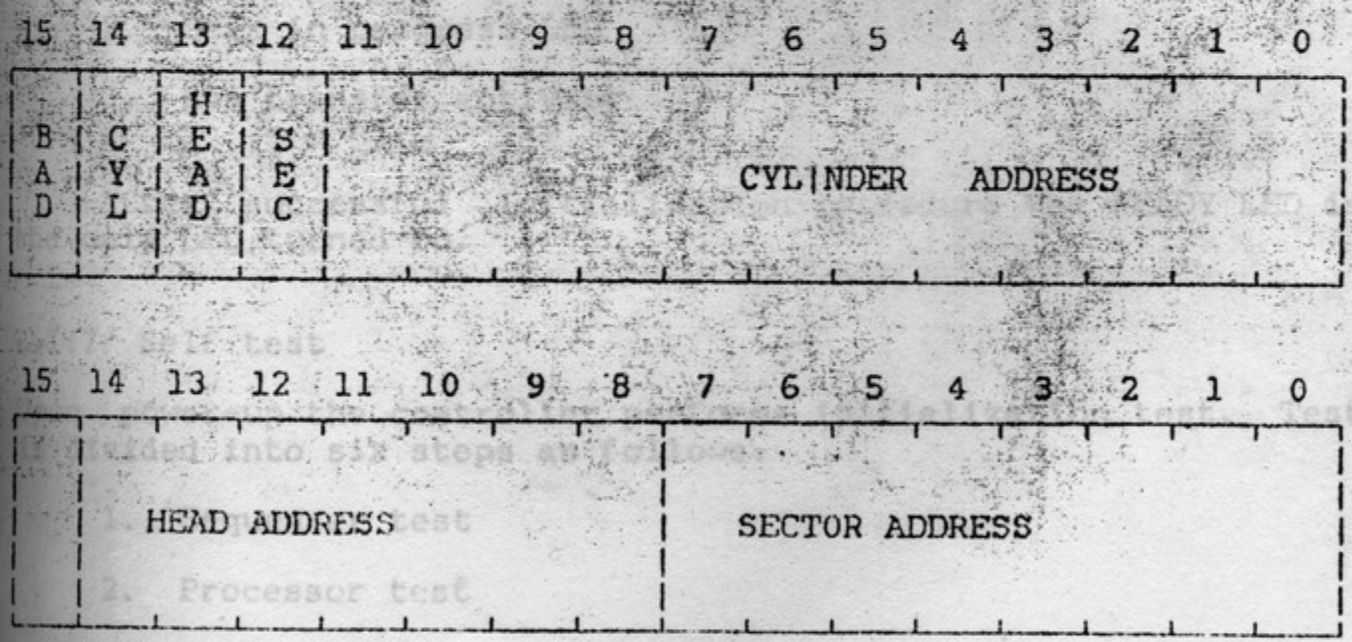
SEGCATPR	SYNC	HEADER DATA	HEADER ECC	HEGAADP	SYNC	SECTOR DATA	DATA ECC	DATA GAP

AREA	BYTES
SECTOR PULSE WIDTH	3(*)
SECTOR GAP	18
SYNC	1
HEADER	4
HEADER ECC	4
HEADER GAP	18
SYNC	1
DATA	512
DATA ECC	4
DATA GAP	10
TOTAL	582 + SECTOR PULSE

(*) DRIVE DEPENDANT

2.1.5 Header Format

The ID portion of sector contains four words; two words for header data and 32-bits for ECC pattern.



First word: Cylinder address and flags

BAD -- If set indicating the bad sector

CYL -- Is set for all sectors on all tracks of the last cylinder

HEAD -- Is set for all sectors on the last track of any cylinder

SEC -- Is set for the last sector of any track

Second word: Head and sector address

2.1.6 Indicators

Controller has three LEDs as indicators:

1. Ready LED (controller IDLE)
2. Seek in progress LED
3. Bus transfer activity

After successful initialization procedure the READY LED is the only LED turned on.

2.1.7 Self test

Upon power-up the controller performs initialization test. Test is divided into six steps as follows:

1. Sequencer test
2. Processor test
3. Ram test
4. ECC test
5. Internal register test

6. Device test

If any of these tests fails, controller reports the error in the maintenance status register. The LEDs indicate which test failed as follows:

BUS LED	SEEK LED	READY LED	ERROR
ON	OFF	OFF	Sequencer test failed
OFF	ON	OFF	Processor test failed
ON	ON	OFF	RAM test failed
ON	OFF	ON	ECC test failed
OFF	ON	ON	P-REG test failed
(*) ON	ON	ON	Device Test failed

(*) NOTE: Device test is enabled with the jumper BR1 installed, otherwise the device test is not executed upon power-on.

CHAPTER 3

INSTALLATION

This section describes the step-by-step procedure for installation of the BP-01 Disk Controller. The following is a list of installation steps:

1. Inspect the BP-01
2. Prepare the disc drives
3. Configure the BP-01
4. Install the BP-01
5. Route the drive I/O cables
6. Test the controller

3.1 INSPECTION

Make a visual inspection of the board after unpacking. Check specifically for bent or broken connector pins, damaged components or any other evidence of physical damage.

3.2 DISK DRIVE PREPARATION

The disk drive must be configured for the proper number of sectors and must have the address selection switches properly configured.

3.2.1 Local/Remote

The LOCAL/REMOTE switch controls whether the drive can be powered up from the drive (LOCAL) or the controller (REMOTE).

3.2.2 Sectoring

The disk drive can be configured for any number of sectors per track, depending on the track length.

3.2.3 Drive numbering

An address from 0 to 3 must be selected for each connected drive. Check the technical manual of the drive for the address selection.

3.3 CONFIGURING THE BP-01

Only one configuration setup must be made on the controller before inserting into chassis. This is made by SW1. Figure 3-1 shows an assembly diagram of the BP-01 Controller Board.

3.3.1 Address selection

The Controller have a block of several command and status registers through which the system can command the controller. The block contains 16 registers.

The BP-01 provides one standard and one optional address selectable by switch SW1 as follows:

SW1	Address	
OFF	774000	Standard
ON	774040	Optional

3.3.2 Interrupt Vector Address

The Interrupt Vector Address does not need to be configured. The controller firmware provides the function for loading the Interrupt Vector Address. If the Address is not loaded the controller uses the default Interrupt Vector Address 174(8).

3.4 PHYSICAL INSTALLATION

3.4.1 SPC Slot Selection

The controller may be placed in any SPC slot along the UNIBUS, non regarding the NPR priority. The controller contains adequate buffering to prevent data lates and will automatically release the bus if any other device is waiting for the Unibus.

3.4.2 NPG Signal Jumper

The NPG signal jumper between pins CA1 and CB1 on the backplane must be removed so that the NPG signal passes through the controller

3.4.3 Mounting

The controller board should be plugged into the backplane with components oriented in the same direction as the CPU and other modules. Insert and remove the board with the computer power OFF to avoid damage to the components.

3.5 CABLING

The A and B cable signals are shown in Figure 3-2.

Fig 3-2 SMD 4.5 CABLE SIGNALS

A - CABLE					B - CABLE	
1	-	TAG1	+	31	1	GND
2	-	TAG2	+	32	2	- SCLK
3	-	TAG3	+	33	3	- RDATA
4	-	BUS 0	+	34	4	GND
5	-	BUS 1	+	35	5	- RDCLK
6	-	BUS 2	+	36	6	- WCLK
7	-	BUS 3	+	37	7	GND
8	-	BUS 4	+	38	8	- WDAT
9	-	BUS 5	+	39	9	+ SEL0
10	-	BUS 6	+	40	10	- SKEND
11	-	BUS 7	+	41	11	GND
12	-	BUS 8	+	42	12	
13	-	BUS 9	+	43	13	
14	-	OPN CBL	+	44	14	+ SCLK
15	-	FLT	+	45	15	GND
16	-	SKERR	+	46	16	+ RDATA
17	-	ONCYL	+	47	17	+ RDCLK
18	-	IDX	+	48	18	GND
19	-	RDY	+	49	19	+ WCLK
20				50	20	+ WDAT
21	-	BSY	+	51	21	GND
22	-	USEL TAG	+	52	22	- SEL0
23	-	SEL0	+	53	23	+ SKEND
24	-	SEL1	+	54	24	
25	-	SCT	+	55	25	GND
26	-	SEL2	+	56	26	
27	-	SEL3	+	57		
28	-	WPRT	+	58		
29	-	PICK-HOLD	+	59		
30	-	BUS 10	+	60		

3.5.1 A Cable

The 60-wire A cable should be plugged into the connector on the A port of the controller and wired to the first drive. If more than one drive is used, it is then daisy-chained to the other drives. The last drive on the A cable must have a terminator installed.

3.5.2 B Cable

Each drive must have 26-wire B cable wired from the drive to one of the B ports of the controller. It makes no difference which B port connection is used by the drive. No external terminators are used with the B cable.

3.5.3 Grounding

For proper operation of the disk subsystem, it is very important that the disk drives have a good ground connection to the logic ground of the host computer.

3.6 TESTING

3.6.1 Self-Test

The Controller will automatically execute a built-in power-up self-test. The self-test is executing on every BUS INIT. If the self-test has been executed successfully, the READY LED will be ON. All three LEDs will be ON or flashed when the controller cannot properly address at least one drive. This will occur if the A and/or B cables are not properly plugged in or two drives have an identical code plug.

The following table contains possible states of LED and explanation:

All three LEDs permanent ON	Controller can-not address at least one drive on A cable. The A cable is probably not plugged in or it can be reverse plugged in.
All three LEDs Flashing with high frequency	The Controller detects a reverse connection of B cable(s).
All three LEDs Flashing with low frequency	The Controller detects none of the B cables connected to the B ports of the controller, or none of the drives are powered-on

3.6.2 Register Examination

After powering-up the CPU and READY LED is ON, a check should be made to ensure that the console registers can be read from the computer console. The BPCSR will contain 000040 and all other registers contain 000000.

3.6.3 Hardware Formatting the Disk

The Controller has the capability to format the disk. This format does not verify the data or headers and does not write Bad Sector File. The following instructions are valid to format the drive.

1. Halt the CPU and press INIT
2. Install a scratch pack on the drive 0 and make ready.
3. Deposit the drive number (if other than 0) in BPCS1 at 774006 (774046 if alternate address is selected).
4. Deposit the maximum Cylinder number minus one (cyl - 1) into the BPCYL at 774020 (774060 if alternate address is selected).

5. Deposit the maximum Head and Sector address minus one (head-1,sector-1) into the BPDAD at 774016 (774036 if alternate address is selected).

6. Deposit a 177400 in BPWCT at 774002 (774042 if alternate address is selected).

7. Deposit a 000021 in BPCSR (Format Disk command) at 774000 (774040 if alternate address is selected).

8. Examine BPDSR at 774010 (774050 if alternate address is selected) to see if the drive is in error. The READY LED should flash. BPCYL and BPCSR should be examined to determine the Cylinder currently under format and Controller status.

   At the end of the formatting the READY LED should stop flashing indicating the Controller is in idle state. Examine the contents of BPCSR register to see, if the function has been completed (ERR bit 0).

9. Issue the GDP command (place 000023 into BPCSR) and check the contents of BPCYL and BPDAD registers.

CHAPTER 4

CONTROLLER REGISTERS

4.1 DEVICE REGISTERS

There are 16 device registers in the BP-01 controller. They are used to interface the controller to the drives and the computer. The registers are loaded and/or read under program control in order to initiate selected disk commands and monitor status and error conditions. Registers can be written in only by word operations.

The BPATT register is provided to monitor the status of all four drives at one time.

The following table is a summary of the registers used by the program. The registers are contained in the RAM buffer.

Controller register summary

NAME	ADDRESS	DESCRIPTION
BPCSR	XXXX00	CONTROL AND STATUS
BPWCT	XXXX02	WORD COUNT
BPBAD	XXXX04	UNIBUS ADDRESS 0-15
BPCS1	XXXX06	CONTROL AND STATUS 1
BPDSR	XXXX10	DRIVE STATUS
BPER1	XXXX12	ERROR REGISTER 1
BPATA	XXXX14	ATTENTION REGISTER
BPDAD	XXXX16	HEAD - SECTOR
BPCYL	XXXX20	CYLINDER
BPEC1	XXXX22	ECC POSITION
BPEC2	XXXX24	ECC PATTERN
BPER2	XXXX26	ERROR REGISTER 2
BPTRC	XXXX30	TRANSACTION COUNT
BPCAT	XXXX32	CONTROLLER ATTENTION
BPMNC	XXXX34	MAINTENANCE CONTROL
BPMNS	XXXX36	MAINTENANCE STATUS

4.1.1 Control and Status Register (BPCSR)

Unibus address : xxxx00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR	OFM	OFP	STM	STP		EXBA		BSY	EI	RDY	FUNCTION				GO

Bit 0 : GO
This bit is set by the program to start the controller operation. It is reset when the controller is ready to accept a new command.

Bits 1 - 4 : FUNCTION
The program sets function code to be performed in this field.

Function codes are :

Function code			
Binary	Octal(*)	Hexadecimal(*)	Function description
0000g	00	00	Nop
0001g	02	02	Seek
0010g	04	04	Recalibrate (Home seek)
0011g	06	06	Controller init
0100g	10	08	Read
0101g	12	0A	Write
0110g	14	0C	Read header
0111g	16	0E	Format track
1000g	20	10	Format disk
1001g	22	12	Get drive parameters
1010g	24	14	Load vector
1011g	26	16	Dump controller memory
1100g	30	18	Diagnostic functions

(*) codes include GO bit set to 0.

Bit 5 : Ready (RDY)
Controller ready bit - this is the only bit set after the controller initiation. When set it indicates that the controller is ready for a new command.

Bit 6 : Enable interrupts (EI)
This bit is set or cleared by the program. By setting this bit, program enables the controller to trigger an interrupt when operation is completed.

Bit 7 : Busy (BSY)
This bit is used, together with Lock bit, to synchronize access to device registers between the program and the controller. This bit is set by controller after it fills all registers with data and triggers an interrupt. Program sets this bit before it moves data into device register. When this bit is set, controller will not change contents of the device registers.

Bits 8 and 9 : Extended bus address (EXBA)
The program sets these bits to address bits 16 and 17 of the Unibus address (data buffer address).

Bit 11 : Strobe plus (STP)

Bit 12 : Strobe Minus (STM)
These two bits are used by the program when the read operation is retried. Only one of these two bits may be set at one time. Bit is cleared by the controller after the operation is completed.

Bit 13 : Offset Plus (OFP)
This bit is set by the program and tells the controller to offset the heads from the center line. Bit is cleared by the controller after the operation is completed.

Bit 14 : Offset Minus (OFM)
This bit is set by the program and tells the controller to offset the heads from the center line. Bit is cleared by the controller after the operation is completed. These two bits are used by the program when the read operation is retried. Only one of these two bits may be set at one time.

Bit 15 : Error (ERR)
This bit is set by the controller when any type of error occurred during the operation.

4.1.2 Word Count Register (BPWCT)

Unibus address : xxxx02

This register is used with data transfer operations and is set by the program to determine a length of data transfer. For read and write operations program sets this register to negative number of words of the data to be transferred. For format disk operation program sets this register to negative number of sectors per track, multiplied by 2.

4.1.3 Buss Address Register (BPBAD)

Unibus address : xxxx04

This register is used with data transfer operations and is set by the program to set the starting address of the data buffer in the memory. It is loaded to specify the 16 low order bits at the starting memory address. The register is updated at the completion of the function.

4.1.4 Control and Status Register 1 (BPCS1)

Unibus address : xxxx06

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		M	N	N	P	M		L		I	E	D	H	UNIT	
E		P	X	X	E	X		O		S	C	F	C		
J		R	D	M	R	F		C		M	D	I	I	#	
								K							

Bits 0 and 1 : Unit number
These two bits are set by the program to select a desired disk unit (0 - 3).

Bit 2 : Header compare inhibit (HCI)
When set, the header comparison is inhibit. The contents of the header of the target sector are not validated. If set, the desired sector is always searched from the Index Mark.

Bit 3 : Format data disable (FDI)
When set, indicates that the contents of the formatted sector is left unchanged. Only the header is overwritten.

Bit 4 : ECC disable (ECD)
When set, disables the correction of the corrupted data in the data buffer. The controller actually performs ECC correction routine but it does not perform data correction.

Bit 5 : Interleaved sector map (ISM)

Bit 6 : Reserved

Bit 7 : Lock (LCK)
This bit, together with Busy bit, is used to synchronize access to device registers. This bit is set by controller before it modifies contents of registers, and is cleared by controller, when values of registers are set. This happens before an interrupt is triggered by the controller.

Bit 8 : Unused

Bit 9 : Missed transfer (MXF)
Data miss from disk to controller. Set if no SYNC character is found during a READ or WRITE operation.

Bit 10 : Program error (PER)
This bit is set by controller if the program attempted an illegal operation, or started a legal operation in an illegal way, or the program has set an illegal combination of bits (like setting bits for plus and minus offset simultaneously).

Bit 11 : Nonexistant memory (NXM)
This bit is set by controller indicating the memory transfer missed. The bus address register will contain the address +2 of the memory location that does not exists.

Bit 12 : nonexistent drive (NXD)
Set by controller if an operation is attempted to nonexistent drive.

Bit 13 : Unibus parity error (UPE)
Set by controller when a memory parity error occurs.

Bit 14 : Unused

Bit 15 : Operation Rejected (REJ)
Set by the controller, indicating an operation request to a drive, while the controller is already performing another operation on the same drive.

4.1.5 Drive Status Register (BPDSR)

Unibus address : xxxx10

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR	PIP	MON	WLK				DBSY	DRDY	OFA						

Bits 0 through 5 : Unused

Bit 6 : Offset mode active (OFA)
Set by the controller, indicating that offset mode operation is active.

Bit 7 : Drive ready (DRDY)
Indicates the drive is ready and on line. This bit is set by the controller after the "Get drive parameters" function has been issued for a ready disk drive.

Bit 8 : Drive busy (DBSY)
When set, indicates that the controller is already performing an operation on the selected drive.

Bits 9 through 11 : Unused

Bit 12 : Disk write locked (WLK)
This bit is set by the controller, when the drive is write locked and a write or format operation is attempted.

Bit 13 : Media online (MON)
Set by the controller, indicating the drive is physically connected to the controller.

Bit 14 : posittioning in progress (PIP)
Set by the controller, when performing the positioning operation on the selected drive.

Bit 15 : Error (ERR)
Set by the controller. This bit is set when an error occurs on selected drive.

4.1.6 Error Register (BPER1)

Unibus address : xxxx12

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR2	SLE	BDS	SIC	DTC	DVC	OPI	WLE	IVA	OVF	HEC	HCE	ECH	RCF	WCF	ILF

Bit 0 : Illegal function (ILF)
Set by the controller. The function code is not legal.

Bit 1 : Write clock failed (WCF)
Set by the controller. The controller is unable to write the current sector.

Bit 2 : Read clock failed (RCF)
Set by the controller. The controller is unable to read

data from the disk drive.

Bit 3 : ECC hard error (ECH)
Set by the controller when an unrecoverable ECC error was detected.

Bit 4 : Header compare error (HCE)
Set by the controller. The sector address is not as expected.

Bit 5 : Header ECC error (HEC)
Set by the controller when an ECC error occurs during read sector header. It causes a current function to terminate without transferring any data from/to the disk.

Bit 6 : Disk address overflow (OVF)
Set by the controller when the seek operation is initiated with cylinder address greater than the real number of cylinders on the selected drive.

Bit 7 : Invalid address (IVA)
Set by the controller, if the cylinder address is over 1024(10).

Bit 8 : Write lock error (WLE)
Set by the controller indicating the Write protect switch is on on the selected drive during the WRITE or FORMAT operation.

Bit 9 : Operation incomplete (OPI)
Set by the controller indicating that the current operation was not successfully completed due to error conditions.

Bit 10 : Device check (DVC)
Set by the controller indicating an hardware error on selected drive.

Bit 11 : Data check (DTC)
Set by the controller indicating a data error during a READ operation.

Bit 12 : Seek incomplete (SIC)
Set by the controller, indicating a seek failure. Recalibrate function should be issued to the drive.

Bit 13 : Bad sector (BDS)
Set by the controller, indicating that the current sector has a bad flag.

Bit 14 : Select error (SLE)
Set by the controller, indicating that an operation was initiated to the nonexistent drive.

Bit 15 : Error in error 2 register (ER2)
Set by the controller, indicating that a fatal error is in the second error register.

4.1.7 Attention Register (BPATT)

Unibus address : xxxxl4

Contains the attention summary status for all drives. A status for each drive is set after a request to that drive has been issued or diagnostic test has been performed.

15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
DRIVE 3 SUMMARY	DRIVE 2 SUMMARY	DRIVE 1 SUMMARY	DRIVE 0 SUMMARY

There are four status bits provided for each drive.

Bit 1: Drive ready (ATSRDY)
Set, if a drive is ready and online.

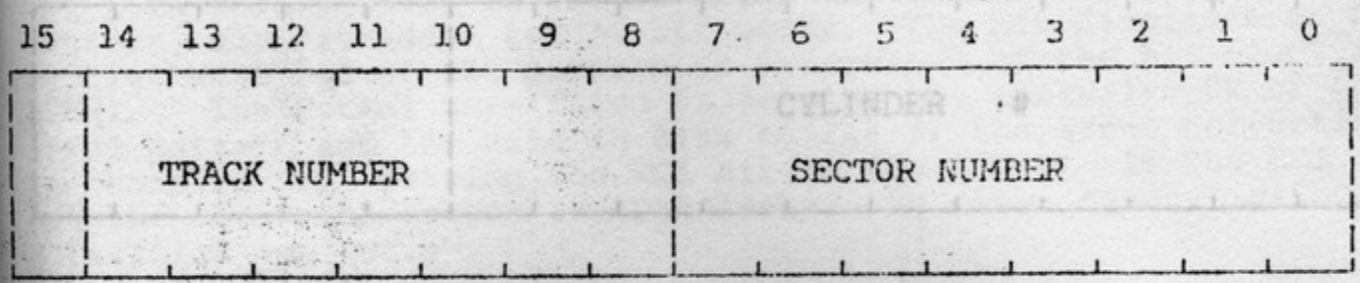
Bit 2: Drive on cylinder (ATSCYL)
Set, if a drive is on cylinder.

Bit 3: Drive in error (ATSERR)
Set, if any error occurred on a drive.

Bit 4: Drive write protected (ATSWLK)
Set, if a drive has write lock switch on.

4.1.8 Disk Address Register (DAR)

Unibus address : xxxxx16



Bits 0 through 7 : Sector number.
The sector number is incremented after each successfully completed function. The sector number can be up to 377(8).

Bits 8 through 14 : Track number.
The track number (head) is incremented after each successfully completed function. The head number can be up to 177(8).

Bit 15 : Reserved.

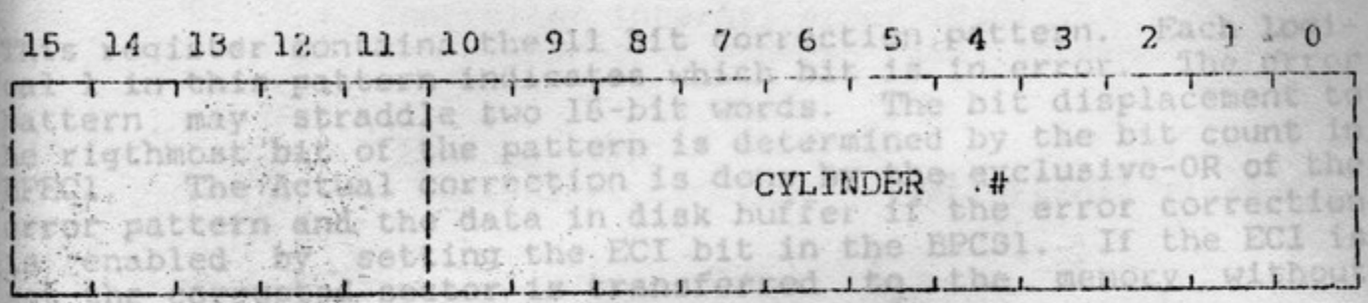
With data transfer and positioning operations this register is set by the program to the desired sector and track number.

With Format Disk operation this register is set by the program to maximum sector and track number (sectors/track - 1 and tracks/cylinder - 1).

With Get Drive Parameters operation this register is set by the controller to maximum sector and track number available (sectors/track - 1 and tracks/cylinder - 1).

4.1.9 Cylinder Address Register (BPCYL)

Unibus address : xxxx20



Bits 0 through 10 : Cylinder number.

Bits 11 through 15 : Unused.

With data transfer and positioning operations this register is set by the program to the desired cylinder number.

With Format Disk operation this register is set by the program to maximum cylinder number (cylinders/disk - 1).

With Get Drive Parameters operation this register is set by the controller to maximum cylinder number available (cylinders/disk - 1).

4.1.10 ECC Position Register (BPEC1)

Unibus address : xxxx22

When the controller performs the ECC correction routine this register contains the bit position of the burst containing an error.

Note that the controller corrects the data buffer before it transfer block to the memory if the ECC correction enable bit is set. If the error is unrecoverable this register contains the value 10040(8).

4.1.11 ECC Pattern Register (BPEC2)

Unibus address : xxxx24

This register contains the 11 bit correction pattern. Each logical 1 in this pattern indicates which bit is in error. The error pattern may straddle two 16-bit words. The bit displacement to he rigthmost bit of the pattern is determined by the bit count in BPEC1. The Actual correction is done by the exclusive-OR of the error pattern and the data in disk buffer if the error correction is enabled by setting the ECI bit in the BPCS1. If the ECI is set the corrupted sector is transferred to the memory without correction applied.

4.1.12 Second Error Register (BPER2)

Unibus address : xxxx26

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IAD	IWC	NFT		TIM	CIE	VEC							ECS	DLT

Bit 0 : Data late (DLT)
Set by the controller when the controller is unable to complete loading data buffer during WRITE operation or transferring data buffer during READ operation while the drive requests a transfer. This is an informational error.

Bit 1 : ECC soft error (ECS)
Set by the controller. The controller sets this bit when a recoverable data ECC error has been found and ECC correction is enabled.

Bits 2 to 7 : Spare

Bit 8 : Illegal vector loaded (VEC)
Set by the controller when an illegal vector value is loaded into the bus address register during the LOAD vector function. A legal vector value is in a range 0 to 774(8).

Bit 9 : controller internal error (CIE)
Set by the controller when an fatal internal error is detected.

Bit 10 : Timeout (TIM)
Set by the controller, indicating an internal Timeout is occurred.

Bit 11 : Spare

Bit 12 : Not formatted drive (NFT)
Set by the controller during the GET Drive Parameters function, if the controller failed to found any formatted header.

Bit 13 : Illegal word count (IWC)
Set by the controller when an illegal word count is loaded for any operation.

Bit 14 : Illegal disk address (IAD)
Set by the controller when a illegal disk address (cylinder, head or sector) is loaded for any operation.

Bit 15 : Spare

4.1.13 Transaction Count Register (BPTRC)

Unibus address : xxxx30

This register contains a transaction counter incremented at a completion of any function.

4.1.14 Controller Internal Status (BPCAT)

Unibus address : xxxx32

This register is read only and contains an information on maintenance purposes.

4.1.15 Controller Maintenance Control Register (BPMNC)

Unibus address : xxxx34

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDN														FUN	

Bits 0 - 2 : maintenance function

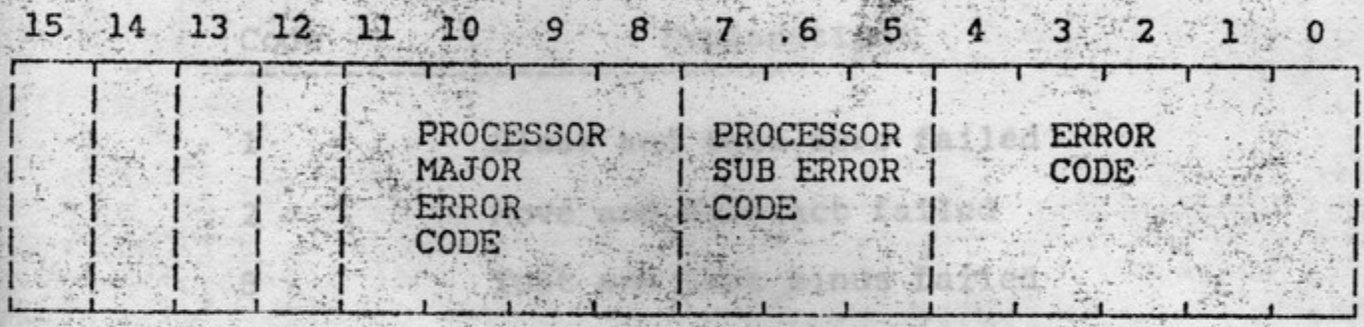
Code	function
001	Sequencer test
010	Processor test
011	RAM test
100	Device test
101	ECC test
110	Internal Registers test
111	Timer test

Bits 3 - 14 : Spare

Bit 15 : Diagnostic function done (DDN)
Set by the controller, indicating the diagnostic function is completed. Must be cleared by the program.

4.1.16 Controller Maintenance Status Register (BPMNS)

Unibus address : xxxx36



Bits 0 - 4 : Error code

Code	Explanation
20	Queue operation failed
21	RAM test failed
22	Sequencer test failed
23	Processor test failed
24	Registers test failed
25	ECC test failed
26	Timer test failed

Bits 5 - 7 : Processor error minor code

Code	Explanation
1	Rotate 1 operation failed
2	Rotate 2 operation failed
4	Shift operation failed

Bits 8 - 11 : Processor error major code

Code	Explanation
1	Clear and test zero failed
2	Move and subtract failed
3	Test and test minus failed
4	AND / OR operations failed
5	Increment failed
6	Decrement failed
7	Shift failed
10	Add and XOR failed

Bits 12 - 15 : Reserved

CHAPTER 5

COMMANDS

5.1 COMMANDS

To initiate an operation program sets proper data, function code and unit number into controller registers; when the program sets go bit in the BPCSR register, the controller reads the registers, clears go bit and initiates the operation. At this point, until the SEEK operation is completed, the controller can accept command for another drive (unit number). The controller is capable of performing one operation on each connected drive simultaneously. However, the controller will reject a command for a busy drive.

When an operation is completed, the controller completes the command by setting final status values into controller registers and triggering an interrupt, if IE bit is set in BPCSR register. The controller completes the commands in the same order as the corresponding positioning operations are completed.

The controller has only one set of registers; the program (when issuing a command) and the controller (when completing a command) are accessing the same set of registers asynchronuosliy. In order to avoid conflicts, both the program and the controller must follow a synchronization procedure to gain exclusive access to the controller registers. Two bits (BSY bit in BPCSR register and LOCK bit in BPCS1 register) are provided for synchronization procedure. The details of synchronization procedure is explained in section 4.2 below.

To initiate an operation the program should

- obtain access to the controller registers by performing the synchronization procedure. (When access is obtained, BSY bit in BPCSR register is set and LOCK bit in BPCS1 register is clear)

- set data, such as unit number, disk address, memory address and word count, into controller registers (but not the BPCSR register).

- set up new contents of the BPCSR register:

  function code

  memory address extension bits

  IE bit with the

  GO bit set

  BSY bit clear

- move the new contents into the BPCSR register.

When an operation is completed (the controller triggers an interrupt), the BSY bit is set and the LOCK bit is cleared by the controller, so there is no need to perform the synchro- nization procedure. The program reads the final status from the controller registers and clears the BSY bit in the BPCSR register (to release access to the registers).

The commands are divided into three categories: data transfer commands, positioning commands and special commands.

5.1.1 Positioning Commands

positioning commands are used to position the heads over the disk pack. Such an action can take milliseconds to complete. The positioning commands are described below:

5.1.1.1 Seek Command - This command causes the heads to be moved to the cylinder address specified by the value in the BPCYL register. If the drive is unable to complete a move within 500 miliseconds or if it has moved the carriage to position outside the recording field, the drive asserts the seek error signal and the controller sets the appropriate status in registers. The controller will not issue any command to clear the seek fault.

5.1.1.2 Recalibrate (Home Seek) - This command will cause the drive possitioner to position the heads over cylinder 0. This command clears drive fault and seek error. This operation is longer than seek to cylinder zero.

5.1.2 Data Transfer Commands

All data transfer commands have seek and sector search functions implied. For all commands except the Format write a match of the sector header must be made before the data transfer is started. If the HCI bit is set, the header will not be compared to the expected value, the transfer will be started based on the pre-recorded sector pulses and no header errors will be reported in case of error. Operation with HCI bit is not recommended because the controller must search for desired sector from the index pulse.

The disc and Unibus address will be automatically incremented after each transferred sector from or to disk. Therefore at the end of function the disc address will contain the address of the next sector. When the cylinder address changes during the transfer, the controller will automatically perform the implied seek.

5.1.2.1 Read Data - This command reads the 256-word data filed from the selected sector and transfers data to the memory. When the sector data transfer (disk to controller) is complete, the ECC is checked to ensure the integrity of data. If a data error occurred, the ECC correction routine is executed to determine whether the error is correctable. If the ECD bit in the BPCS1 is set, the controller will not correct data in the buffer before transferring them to the memory.

5.1.2.2 Read ID - This command transfers the 2-word sector header field for requested number of sectors (up to 127).

5.1.2.3 Write Data - This command writes the 256-word data field of the selected sector. A two word ECC is appended to each sector. If the word count is less than 256 the remaining data are unpredictable (not zero filled). After the sector transfer the disk address is automatically incremented.

5.1.2.4 Format Header and Data - This command writes the 2-word header field obtained from the memory and 256-word data generated in the controller. The data are generated with two fixed word pattern. First word is B6DB(16) second EB6D. A number of the sector to format is computed from BPWCT register using formula sector counter = BPWCT/2.

5.1.3 Special Commands

Special commands are used to initialize the controller, or get the drive characteristics and format disk drive. maintenance commands are special commands.

5.1.3.1 No operation - This command selects drive, reports the drive status into the BPDSR register and clears Unibus address and extension bits.

5.1.3.2 Controller Clear - This command cause the controller to initialize itself and clear all registers, flush the internal queue and set ready bit in BPCSR. This command does not generate interrupt.

5.1.3.3 Load vector - This command is used to load the interrupt vector. The vector value must be supplied in the BPBAD register. Controller checks if the vector is loaded before issuing the interrupt. If the vector is not loaded, the interrupt to default vector (174(8)) will be issued at the end of each command. This command will not generate interrupt itself.

5.1.3.4 Get drive parameters - This command is used to obtain the physical drive size. The drive must be formatted prior to issuing this function. The controller will return the drive physical size into the BPDAD and BPCYL registers. Note that this function can take a significant time to complete at the first time after controller initialization.

5.1.3.5 Format disk - This command is used to format the drive automatically. Note that this command can take a significant time to complete. While this function is active, the controller is not ready to accept the next command for other drives.

5.1.3.6 Dump Ram - This command is used for diagnostic purposes.

5.1.3.7 Maintenance command - This command is used for diagnostic purposes.

5.2 SYNCHRONIZING ACCESS TO DEVICE REGISTERS

If the program tries to access device registers, while the controller is changing register contents, an unpredictable result might appear. The program should follow these rules to synchronize access to the controller registers.

When the controller completes any operation, it will set registers to proper values. To do this, controller first sets Lock bit in the Control ans status register (CSR) and waits for Busy bit clear. Then it updates register contents, clears Lock bit and sets Busy bit; if Enable interrupt bit is set, it triggers an interrupt.

The program should follow the following procedure: before it tries to access controller registers, it sets Busy bit and checks the Lock bit in Control and status register (CSR). If Lock bit is set, the program clears Busy bit and waits for an interrupt.

If Lock bit is clear, the program has an access to controller registers. The program then sets all desired values into registers and clears Busy bit by loading new function code in BPCSR register.

NOTE

Use of read-modify-write instructions is not recommended.

When interrupt occurs, the controller already sets Busy bit, so the program does not need to do that. But the program should clear this bit after it finishes servicing the interrupt.

CHAPTER 6

DIAGNOSTICS

The BPFMT formatter-diagnostic is a stand-alone program intended as a preliminary formatting program and test tool. The BPFMT is distributed in a bootable format.

This chapter describes the use of the BPFMT program. It is assumed the familiarity with the BP-01 controller, as well as the boot procedures.

6.1 INVOKING THE BPFMT

BPFMT can be booted by hardware from the magnetic tape or by software BOO command from the disk media. When the program initializes itself the following message will be displayed:

BP-01 Formatter-Diagnostic program v1.0

6.2 BPFMT COMMANDS

After initialization the program sets the default values for the various symbols which are used to control the operation such as disk-type,interrupt address etc.

The following is the table of the symbols which can be displayed and changed. Initial values are in square brackets.

BRK [0] ASCII code for the break character. Typing this character causes the current operation to abort.

CSESC Current number of sectors to transfer. Must be set before READ or WRITE function.

CYL	Current Cylinder number
DRIVE [0]	Current Drive number. Can be in range from 0 to 3.
HEAD	Current Head number.
INTAD [174]	controller interrupt vector address.
NCYLS	Number of Cylinders on device. This value is set automatically if TYPE is nonzero.
NHDS	Number of Heads on device. This value is set automatically if TYPE is nonzero.
NSECS	Number of Sectors on device. This value is set automatically if TYPE is nonzero.
RBUF	Buffer for reading data.
REP [1]	Routine invocation repeat count
SECT	Current Sector number.
TYPE [1]	Device type number. This value can be modified to other drive type or zero.
UADD [174000]	Controller CSR base address
WBUF	Buffer for writing.

Memory and symbol examination and modification is similar to the Online Debugger. Each line begins with a'>' prompt.

The following is a list of the general rules:

- All numerical data is in octal representation
- expresssions may be used to expres location to be open
- Expressions are evaluated left to right and may contain both numbers and symbols

- Valid operators are [+,-,&,!] (plus,minus,and,or)
- Any illegal input is flagged with a '?'

There are two command characters:

[/] (slash) Open memory location

[<ESC>] (escape) Start routine

6.2.1 Open memory location

Opening memory and modifying it are just like in ODT. To open a location, type the address followed by a slash. BPFMT will show the contents and will wait for input or terminator. If the value is then typed, that value will be stored into the open location.

Terminators are

<LF> (linefeed) open following location

<CR> (carriagereturn) begin new line with prompt

[?] (question-mark) reopen the same location again

[^] (circumflex) open previous location

6.2.2 Start routine - ESCAPE

Routines are started through typing the routine number terminated by the ESCAPE character. The following is a list of routines:

Number	Routine	Description
0	MAIN	Full format and check
1	INITC	Initialize the controller
2	REZT	Home seek
3	SEEKT	Seek test
4	TRK0	Format track zero

5	RW	Read/Write pass over disk
6	WDAT	Write data
7	RDAT	Read data
10	FMT	Format disk - track format
11	SHAKE	Random seeks under interrupts
12	FLAG	Flag bad sectors on disk
13	WALK	Walk through the registers
14	WBOT	Write boot block
15	FMT2F	Format drive
16	GDPT	Get drive parameters

6.2.3 Addresing the controller CSRs

prefixing an expression by ";" causes the base address of the CSRs to be added to that expression. For example ";6" is the Command and Status-1 register and ";12" is the Error-1 Register.

6.2.4 Addresing the saved controller CSRs

BPFMT keeps copy of the controller registers into internal memory. This is useful for examining controller register setting prior to function execution.

preffixing an expression by "*" causes the virtual base address of the saved CSRs to be added to that expression. For example "*6" is the Command and Status-1 register and "*12" is the Error-1 Register.

6.2.5 Printing an expresion value

After a prompt, an expression may be typed followed by an equal sign.

6.3 DRIVE TYPES

The formatter must be configured to operate on the drive at hand since many different models can be connected to the controller.

Symbol TYPE contains an information on the type of the drive. If the TYPE contains zero, the BPFMT will not load physical characteristics (sectors, heads and cylinders) automatically.

The following is the table of drive types and symbol names

F160	Fujitsu 160MB
F300	Fujitsu 300MB
F640	Kentronix 640MB
EAGLE	Fujitsu EAGLE 460MB
NEC1	NEC 500MB
AX40	Ampex 40MB
AX80	Ampex 80MB

6.4 FORMATTING A DISK

6.4.1 Preparation

Boot the formatter and set the type location appropriately. Be sure that the controller is plugged in. The drive must be configured to the same number of sectors as the BPFMT for the specific drive. To inspect the BPFMT internal table start Home seek test and examine locations NCYLS, NHDS and NCESC for that drive type.

6.4.2 Formatting

There are three ways to format the disk pack:

1. Invoke Full format and check routine, the pack will be first tested then formatted, checked for bad sectors and formatted again. This operation can be quite time-consuming for large capacity devices.

2. Invoke routines 0 to 4 to check the disk, then start the FMT routine. This routine formats a pack track by track and checks for validity.

3. Invoke routines 0 to 4 to check the disk, then start a FMT2F routine. This routine will start controller routine to format a pack and will not check the contents of the formatted data. You can start the routine FLAG 12 to scan the pack for bad sectors.

6.5 ERROR MESSAGES

Keyboard interrupt. (BP.CSR/PC)

Break character hit during the operation.

Error after init. (BP.CSR/'ERROR')

The controller is not properly initialized.

Software timeout, function not completed (BP.CSR/'BUSY')

The function was not completted in the expected interval.

Drive not ready. (BP.DSR/'READY')

Drive not present not ready or in error.

Error bit ON. (BP.CSR/'ERROR')

Function terminated with error.

BUSY bit not cleared by INIT. (BP.CSR/'BUSY')

Initialization was not successful.

Bootstrap written to drive 0.

This is an informational message.

BUSY bit OFF. (BP.CSR/'BUSY')

Function never done.

Software detected error. (Read/Expected)

Data read not as written.

Software timeout, no interrupt. (STATUS)

interrupt never came.

Idle, BUSY bit ON (BP.CSR/'BUSY')

Invalid bit setting after IDLE function.

Illegal function not detected. (BP.CSR/'STATUS')

Controller was unable to detect the illegal function.

Compare error. (Read/Expected)

The read data was not as expected.

Invalid BP.CSR value after INIT (BP.CSR)

Initialization unsuccessful.

Bad sector found, cannot flag. (CYL/HEAD/SECTOR)

Sector remains unflagged.

Cannot read memory location (OFFSET)

Controller registers not present.

Cannot write memory location (OFFSET)

Controller registers not present.

No response on unibus (DEV ADDR)

Controller registers not present.

No interrupt in 1 msec. (BP.CSR)

Controller does not respond after an interval.

Unsolicited interrupt. (BP.CSR)

Unexpected interrupt from the controller.

Hardware/Software version

Report on versions.

Program error. (PC/PS)

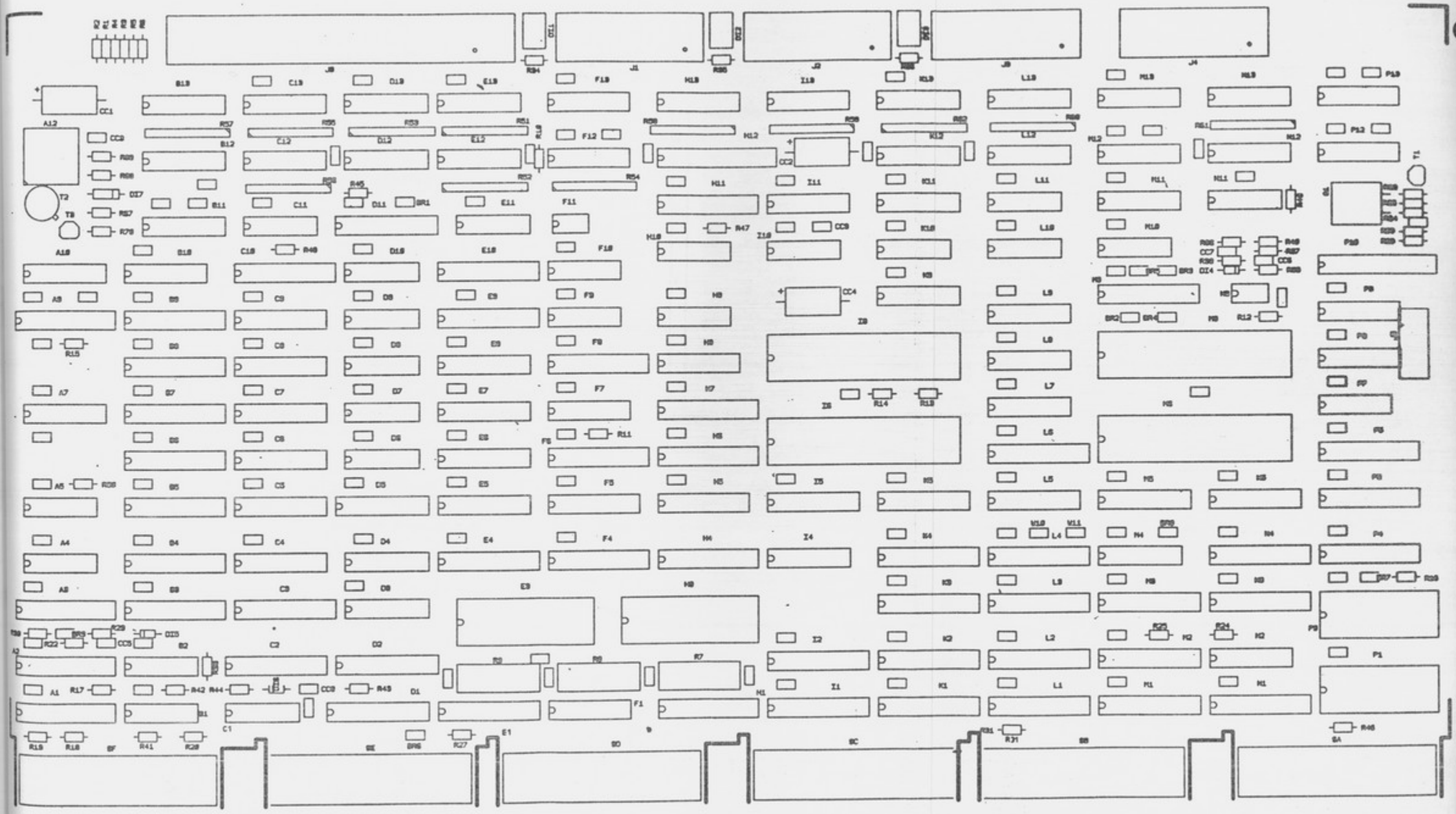
Memory trap during read/write or other trap.

Bad sectors flagged =

This is the informational message.

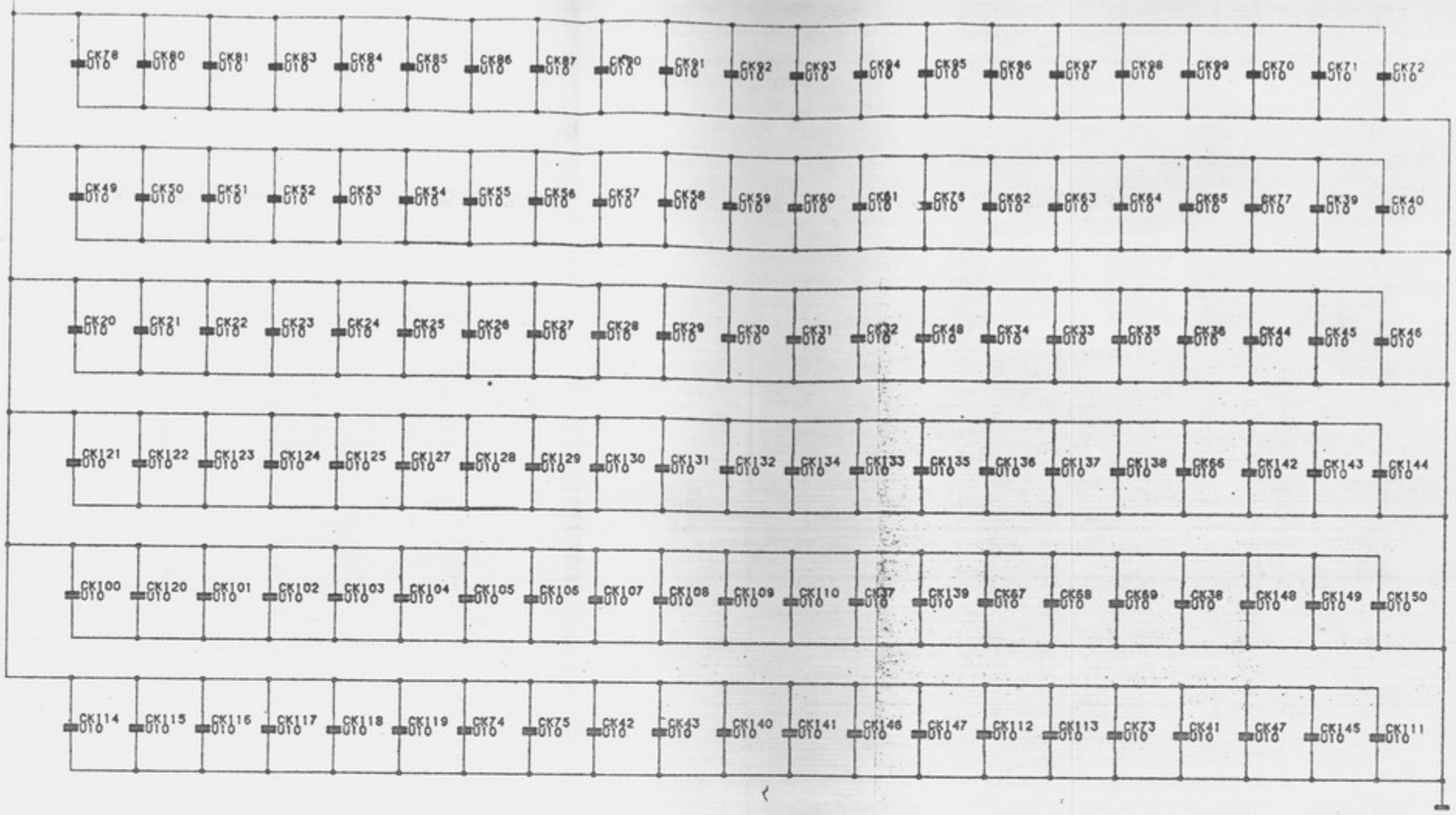
Bad sector flagged. (CYL/HEAD/SECTOR)

This is the informational message.



PLATINENMASS 398,6 X 214,3 MM

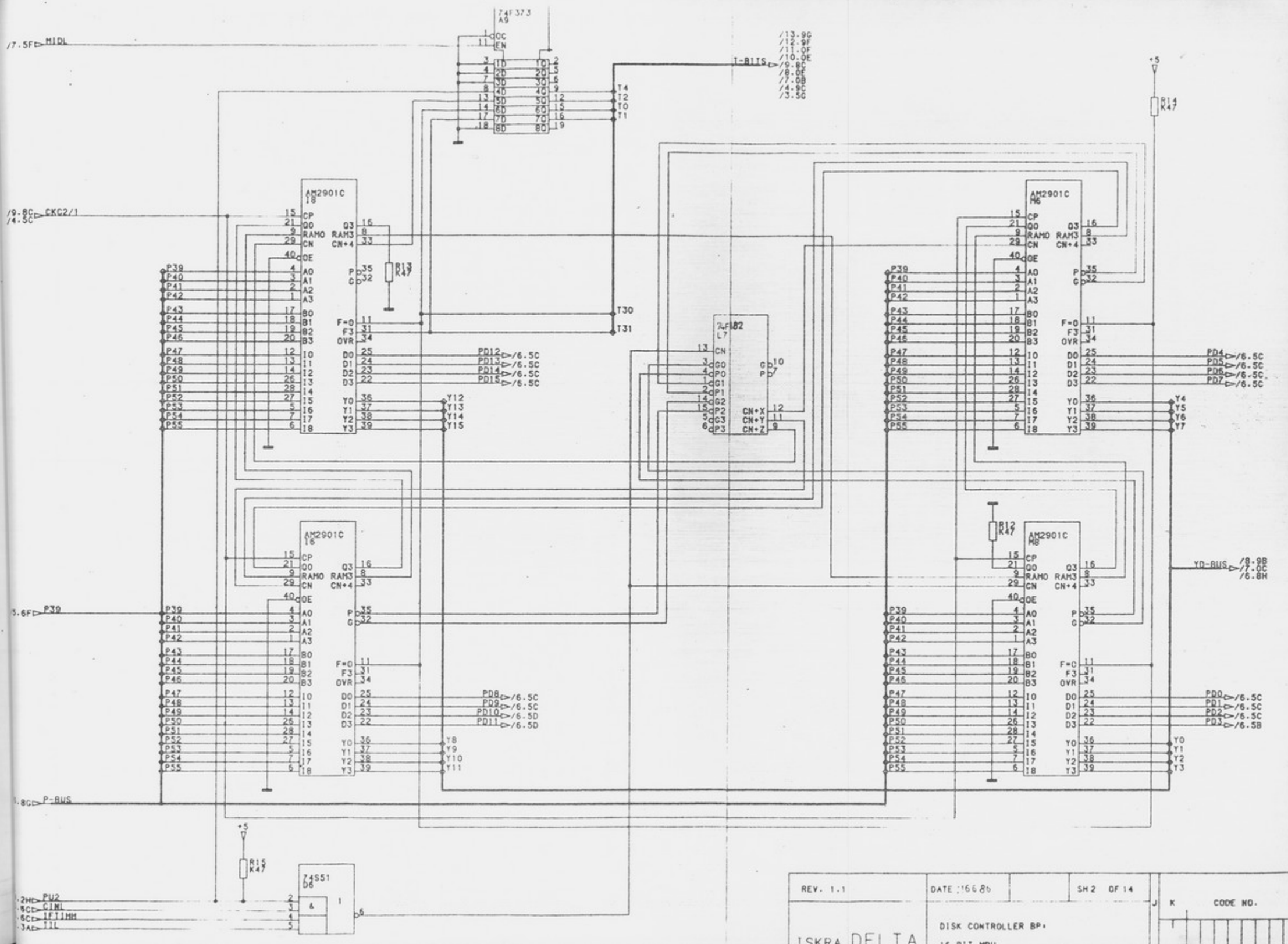
CADE 110485 DJ09/1 SERVICE

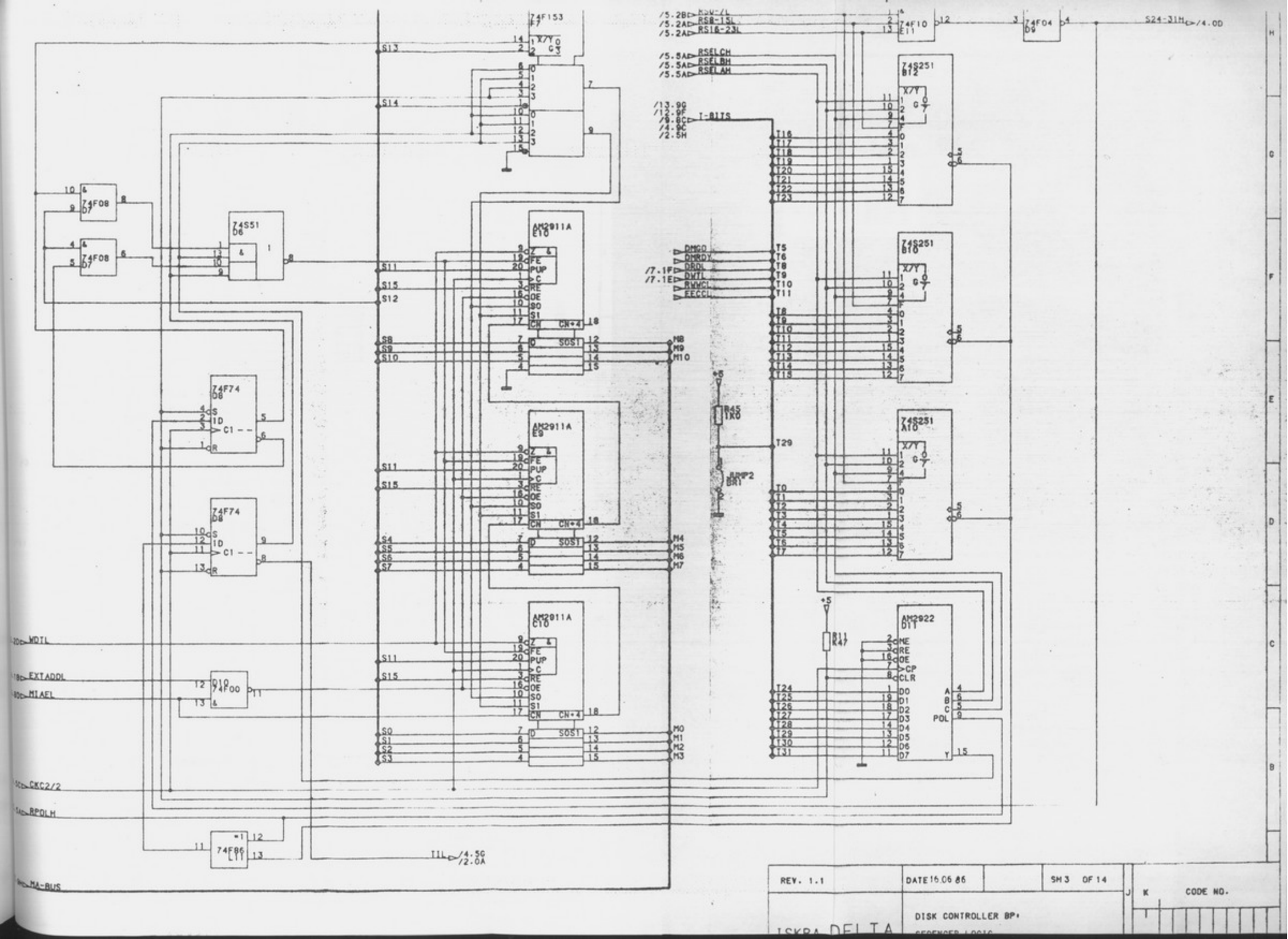


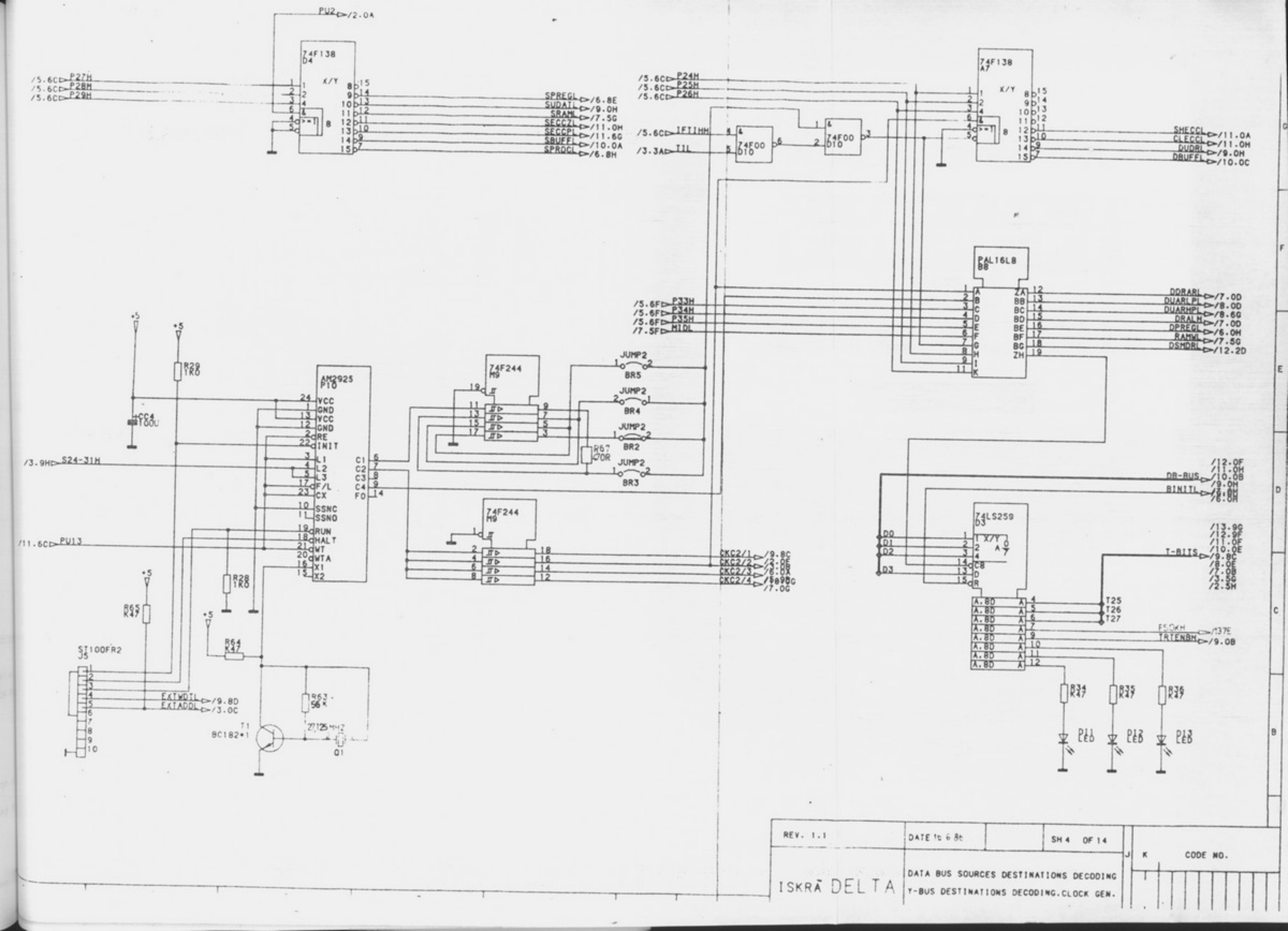
REV. 1.1	DATE		SH OF	K CODE NO
ISKRA DELTA				

1 2 3 4

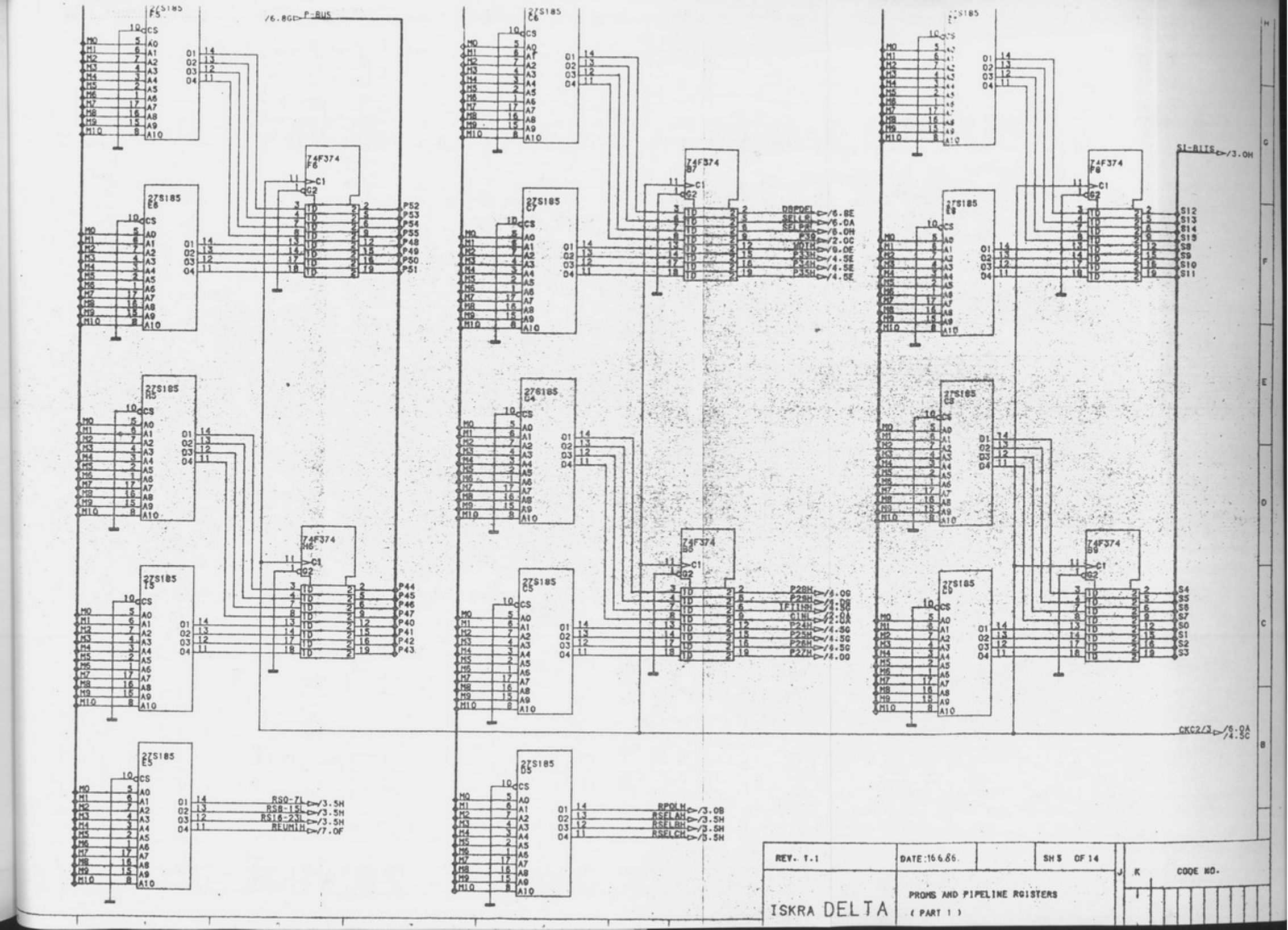
G F E D C B

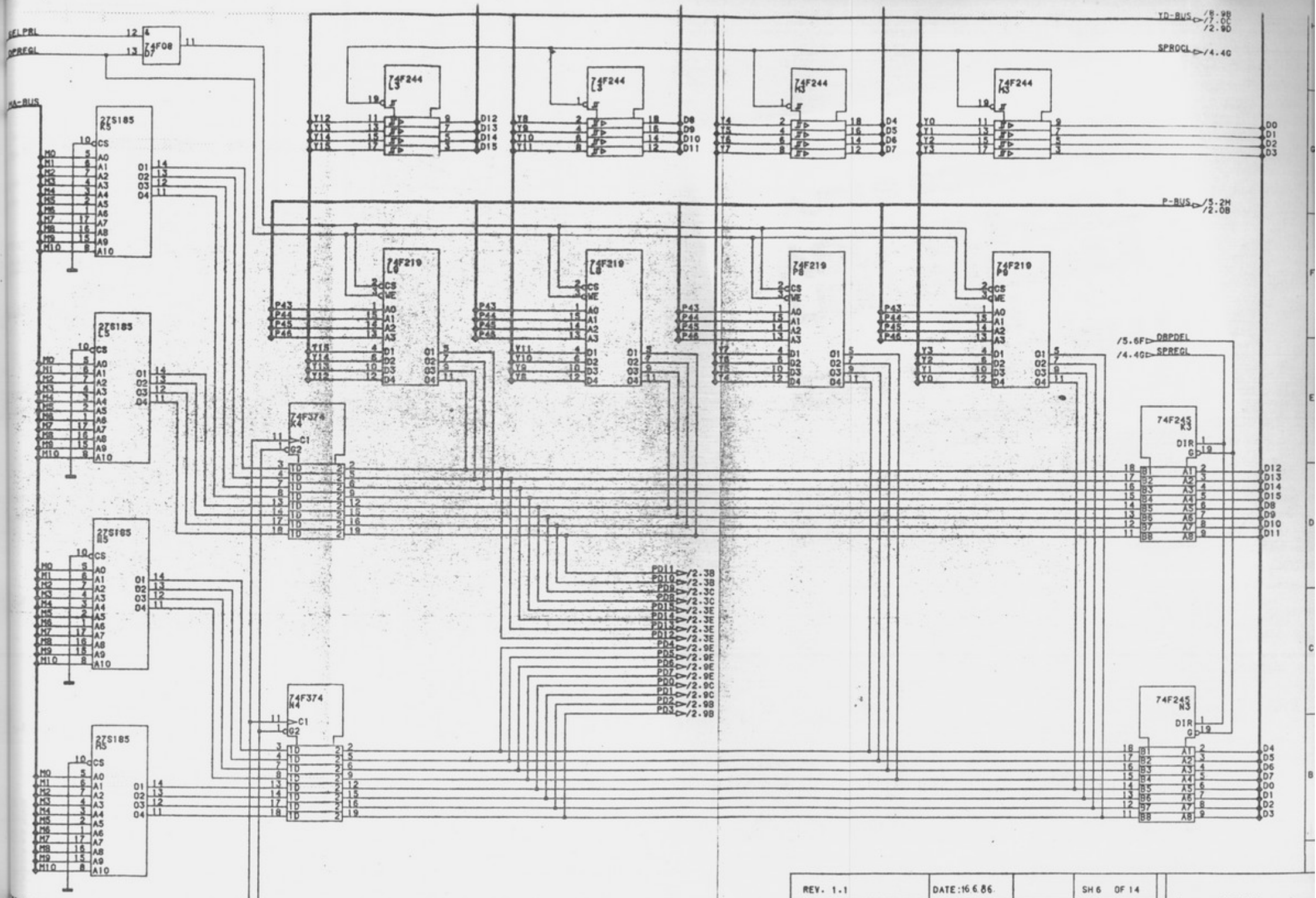

/7.5F MIDL
74F373 A9
T-BITS
/13.9G /12.9F /11.0F /10.0E /9.8C /8.0E /7.0B /4.9C /3.5G
T4 T2 T0 T1
+5
R14 K47
/9.8C /4.5C CKC2/1
AM2901C I8
AM2901C M6
AM2901C I6
AM2901C M8
P39 P40 P41 P42 P43 P44 P45 P46 P47 P48 P49 P50 P51 P52 P53 P54 P55
R13 K47
R12 K47
T30 T31
74F182 L7
PD12 PD13 PD14 PD15 /6.5C
PD4 PD5 PD6 PD7 /6.5C
PD8 PD9 /6.5C PD10 /6.5D PD11 /6.5D
PD0 PD1 PD2 /6.5C PD3 /6.5B
Y12 Y13 Y14 Y15
Y4 Y5 Y6 Y7
Y8 Y9 Y10 Y11
Y0 Y1 Y2 Y3
YD-BUS /8.9B /7.0C /6.8M
5.6F P39
1.8G P-BUS
R15 K47
74S51 D6
2MD PU2
6C CINI
6C IFTIMM
3A TIL
REV. 1.1
DATE 16.6.86
SH 2 OF 14
ISKRA DELTA
DISK CONTROLLER BP+
16 BIT MPU
CODE NO.


REV. 1.1
DATE 16.06.86
SH 3 OF 14
CODE NO.
DISK CONTROLLER BP+
ISKRA DELTA



REV. 1.1	DATE 1c 6 8t		SH 4 OF 14
ISKRA DELTA	DATA BUS SOURCES DESTINATIONS DECODING Y-BUS DESTINATIONS DECODING. CLOCK GEN.		CODE NO.


/6.8G P-BUS
F5 27S185
F6 74F374
E6 27S185
H5 27S185
H6 74F374
I5 27S185
E5 27S185
RS0-7L /3.5H
RS8-15L /3.5H
RS16-23L /3.5H
REUMIH /7.0F
C6 27S185
B7 74F374
C7 27S185
DSPDEL /6.8E
SELLR /6.0A
SELPR /6.0H
P39 /2.0C
WDTH /6.0E
P33H /4.5E
P34H /4.5E
P35H /4.5E
D4 276185
B5 74F374
C5 27S185
P28H /6.0G
P29H /6.0B
IFTIHN /4.5G
G1HL /2.0A
P24H /4.5G
P25H /4.5G
P26H /4.5G
P27H /4.0G
D5 27S185
RPOLH /3.0B
RSELAH /3.5H
RSELBH /3.5H
RSELCH /3.5H
E8 27S185
F8 74F374
SI-BLIS /3.0H
E9 27S185
C8 27S185
D9 74F374
C9 27S185
CKC2/3 /6.0A /4.5C
REV. 1.1
DATE: 16.6.86
SH 5 OF 14
ISKRA DELTA
PROMS AND PIPELINE REGISTERS
(PART 1)
CODE NO.



REV. 1.1	DATE: 16.6.86.		SH 6 OF 14
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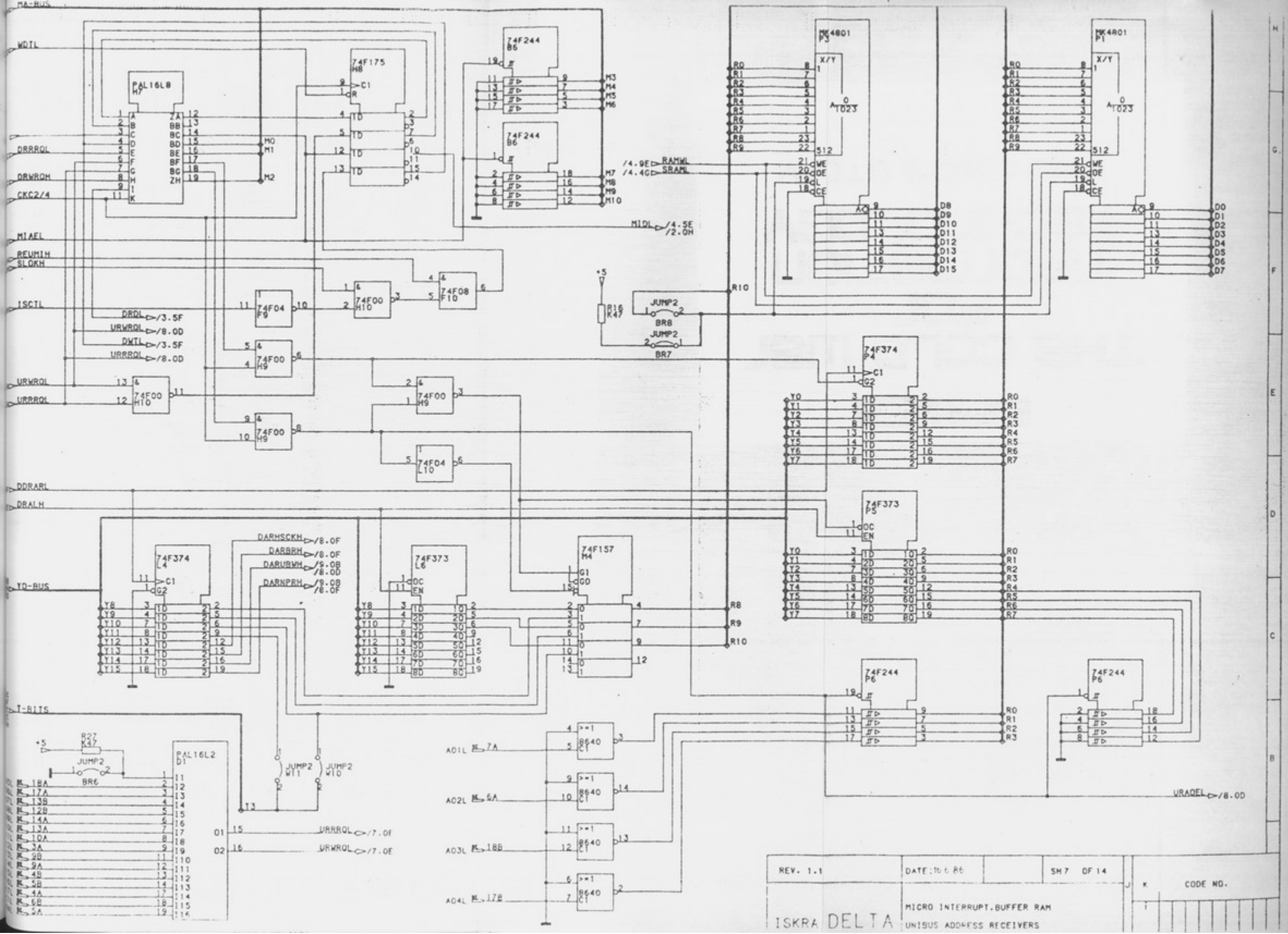
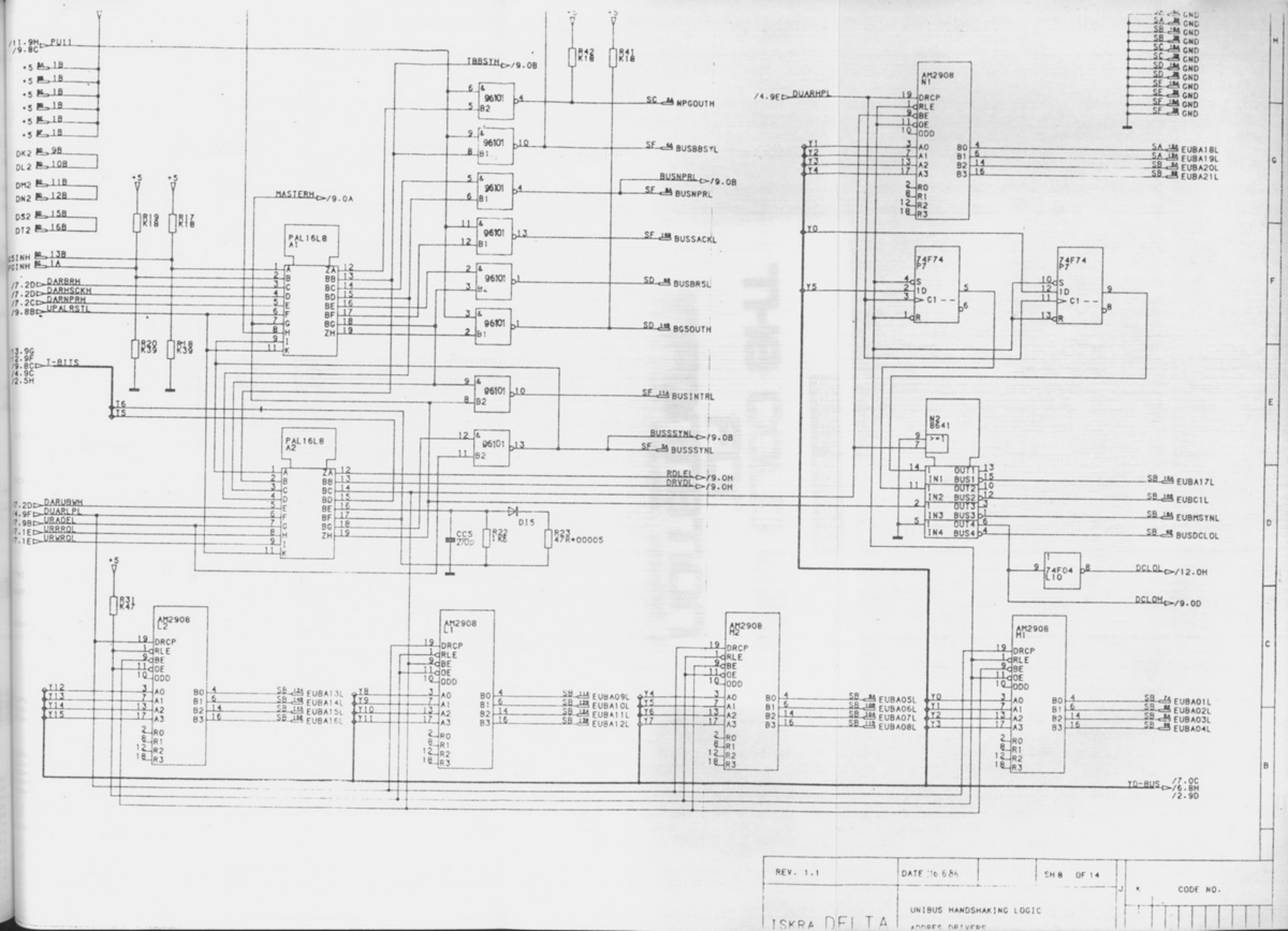
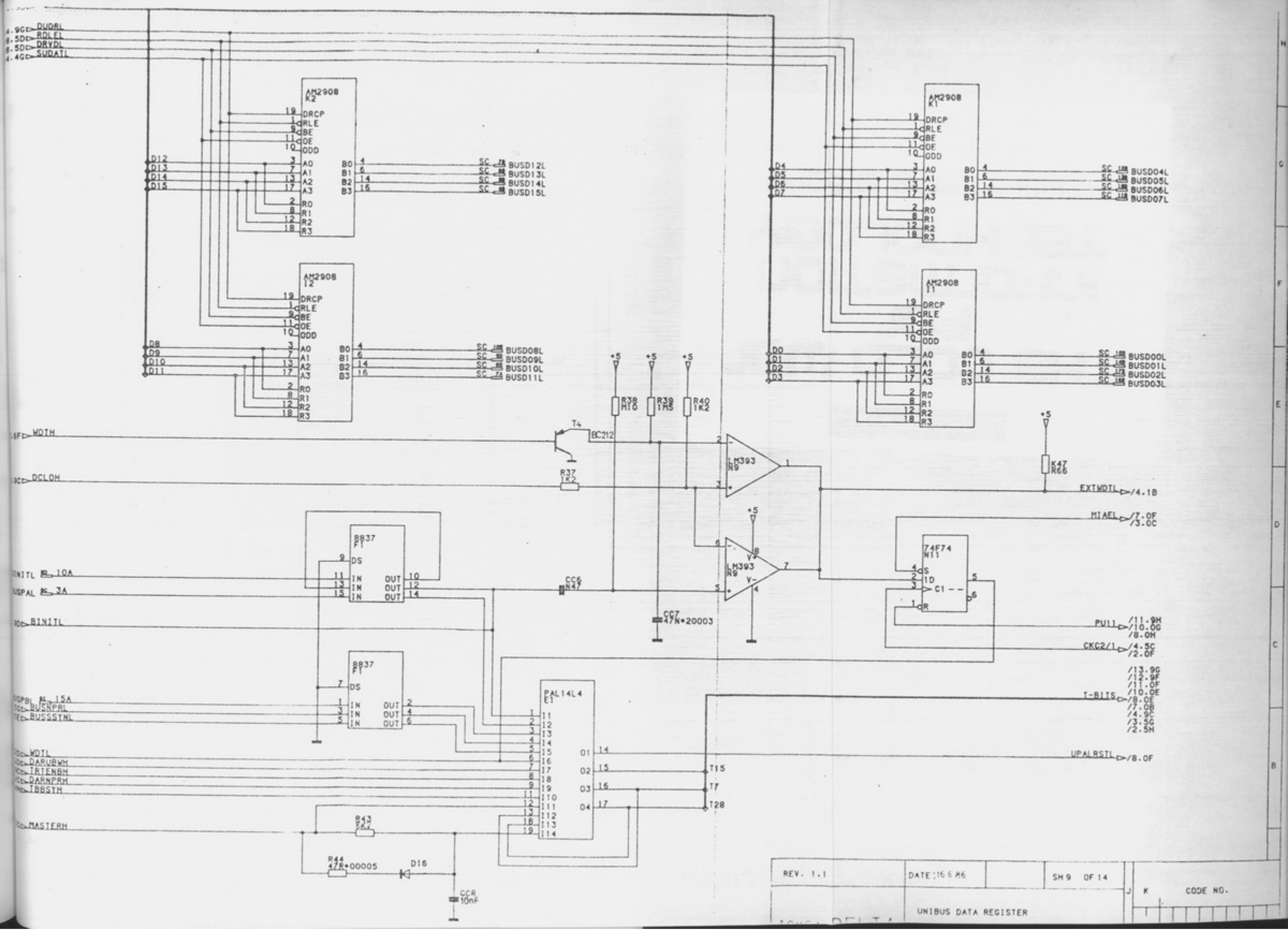
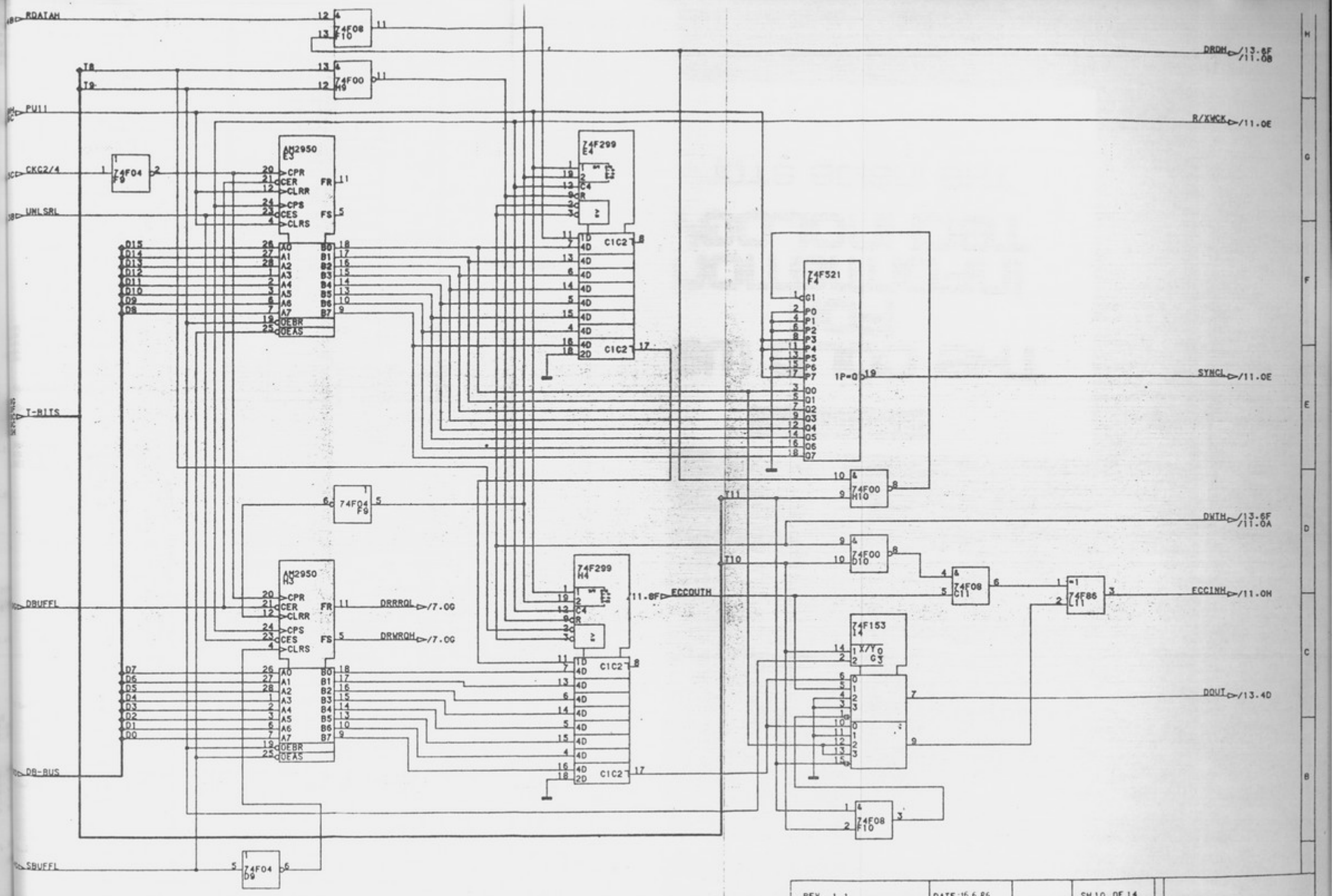

MA-BUS
WDTL
DRRRQL
DRWRQH
CKC2/4
MIAEL
REWMIH
SLOKH
ISCIL
DRDL /3.5F
URWRQL /8.0D
DWTL /3.5F
URRRQL /8.0D
URWRQL
URRRQL
DDRARL
DRALH
YD-BUS
T-BITS
PAL16L8 H7
PAL16L2 D1
74F175 H8
74F244 B6
74F244 B6
74F00 H10
74F00 H9
74F00 H9
74F00 H10
74F00 H9
74F04 F9
74F04 L10
74F08 F10
74F374 L4
74F373 L6
74F157 H4
74F374 P4
74F373 P5
74F244 P6
74F244 P6
MK4801 P3
MK4801 P1
X/Y
1023
512
RAMWL
SRAML
/4.9E
/4.4G
M1DL /4.5E /2.0H
JUMP2 BR8
JUMP2 BR7
R16 K47
R27 K47
JUMP2 BR6
JUMP2 W11
JUMP2 W10
DARHSCKH /8.0F
DARBRH /8.0F
DARUBWH /8.0B /8.0D
DARNPRH /8.0B /8.0F
A01L
A02L
A03L
A04L
8640
URRROL /7.0F
URWROL /7.0F
URADEL /8.0D
REV. 1.1
DATE: 16 6 86
SH 7 OF 14
CODE NO.
ISKRA DELTA
MICRO INTERRUPT BUFFER RAM
UNIBUS ADDRESS RECEIVERS

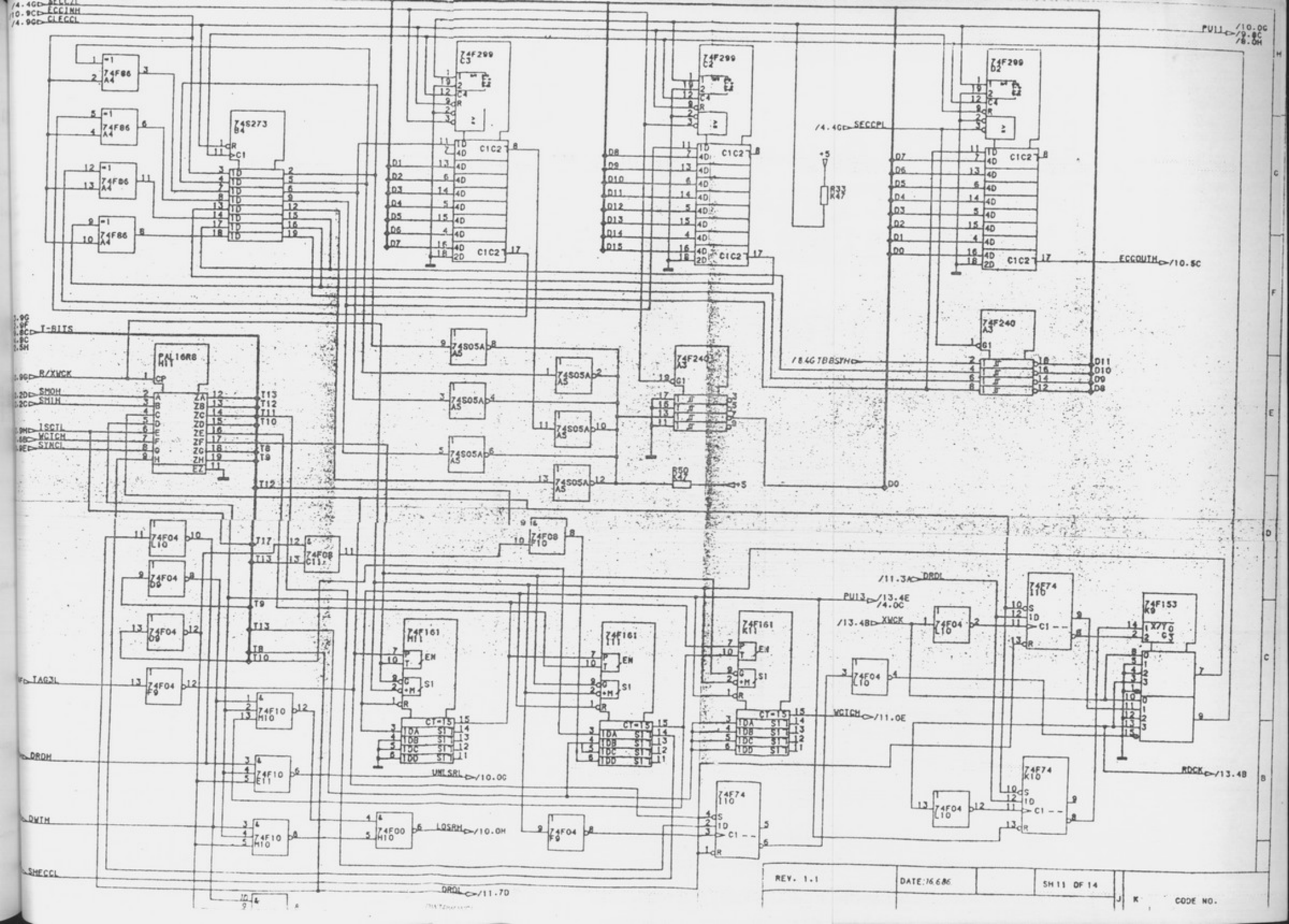


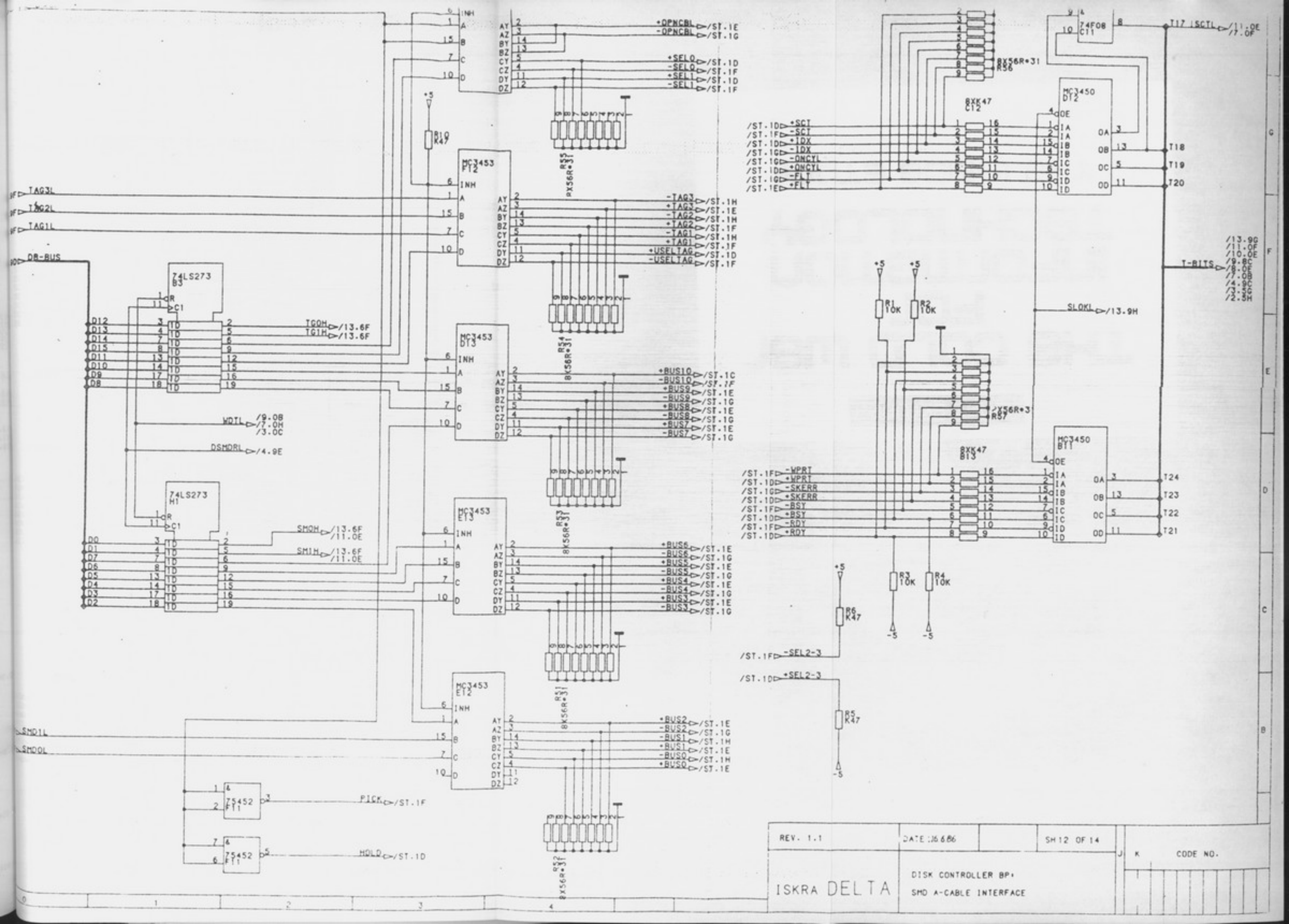
REV. 1.1	DATE 16.6.84	SH 8 OF 14	CODE NO.
ISKRA DELTA	UNIBUS HANDSHAKING LOGIC ADDRES DRIVERS		

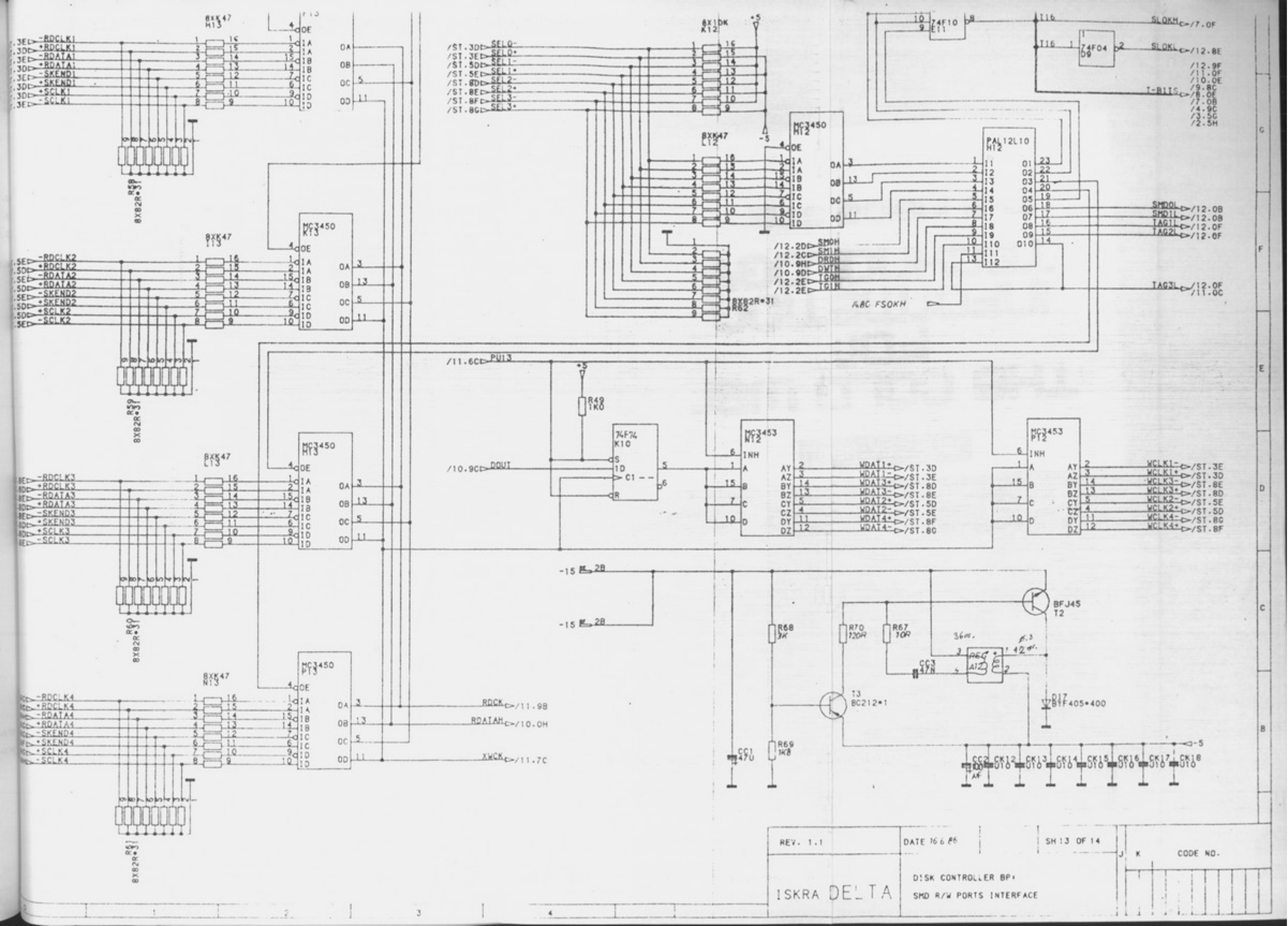


REV. 1.1	DATE: 16 6 86		SH 9 OF 14
UNIBUS DATA REGISTER			CODE NO.


RDAIAH
T8
T9
PU11
CKC2/4
UNLSRL
T-BITS
DBUFFL
DB-BUS
SBUFFL
74F08 F10
74F00 H9
74F04 F9
AM2950 E3
AM2950 H3
74F299 E4
74F299 H4
74F521 F4
74F00 H10
74F00 D10
74F08 C11
74F86 C11
74F153 I4
74F04 F9
74F04 D9
74F08 F10
CPR
CER
CLRR
CPS
CES
CLRS
FR
FS
OEBR
OEAS
D15
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
DRRRQL /7.0G
DRWRQH /7.0G
11.8F
ECCOUTH
T11
T10
1P=0
DRDH /13.6F /11.0B
R/XWCK /11.0E
SYNCL /11.0E
DWTH /13.6F /11.0A
ECCINH /11.0H
DOUT /13.4D
REV. 1.1
DATE:16.6.86
SH 10 OF 14
CODE NO.
READ/WRITE SHIFT REGISTER.SYNC PATERN
ISKRA DELTA


/4.4G ECCCPL
/10.9C ECCINH
/4.9G CLECCL
74F86 A4
74S273 B4
74F299 C3
74F299 C2
74F299 D2
PU11 /10.0G /9.8C /8.0H
/4.4G SECCPL
R33 K4
ECCOUTH /10.5C
74F240 A3
/84GTBBSTH
T-BITS
PAL16R8 H11
R/XWCK
SMOH
SMIH
1SCTL
WCTGH
SYNCL
74S05A A5
R50 J4
74F04 L10
74F04 D9
74F04 C11
74F08 F10
74F08 C11
74F04 F9
74F10 H10
74F10 E11
74F10 H10
74F00 H10
74F161 H11
74F161 J11
74F161 K11
CT=15
UNLSRL /10.0G
LOSRH /10.0H
74F74 I10
74F74 K10
74F153 K9
/11.3A DRDL
PU13 /13.4E /4.0C
/13.4B XWCK
WCTGH /11.0E
RDCK /13.4B
TAG3L
DRDH
DWTH
SHECCL
DRDL /11.7D
REV. 1.1
DATE: 16.6.86
SH 11 OF 14
CODE NO.


MC3453 FT2
MC3453 DT3
MC3453 ET3
MC3453 ET2
74LS273 B3
74LS273 H1
MC3450 DT2
MC3450 BT1
74F08 C11
8XK47 C12
8XK47 B13
Z5452 FT1
Z5452 FT1
8X56R+31
8XK56R+3
R1 10K
R2 10K
R3 10K
R4 10K
R5 K47
R6 K47
DB-BUS
TAG3L
TAG2L
TAG1L
WDTL /9.0B /7.0H /3.0C
DSMDRL /4.9E
SMDH /13.6F /11.0E
SMDL /13.6F /11.0E
SMD1L
SMD0L
TG0H /13.6F
TG1H /13.6F
PICK /ST.1F
HOLD /ST.1D
+OPNCBL /ST.1E
-OPNCBL /ST.1G
+SELO /ST.1D
-SELO /ST.1F
+SEL1 /ST.1D
-SEL1 /ST.1F
-TAG3 /ST.1H
+TAG3 /ST.1E
-TAG2 /ST.1H
+TAG2 /ST.1F
-TAG1 /ST.1H
+TAG1 /ST.1F
+USELTAG /ST.1D
-USELTAG /ST.1F
+BUS10 /ST.1C
-BUS10 /ST.1F
+BUS9 /ST.1E
-BUS9 /ST.1G
+BUS8 /ST.1E
-BUS8 /ST.1G
+BUS7 /ST.1E
-BUS7 /ST.1G
+BUS6 /ST.1E
-BUS6 /ST.1G
+BUS5 /ST.1E
-BUS5 /ST.1G
+BUS4 /ST.1E
-BUS4 /ST.1G
+BUS3 /ST.1E
-BUS3 /ST.1G
+BUS2 /ST.1E
-BUS2 /ST.1G
-BUS1 /ST.1H
+BUS1 /ST.1E
-BUS0 /ST.1H
+BUS0 /ST.1E
+SCT
-SCT
+IDX
-IDX
-ONCYL
+ONCYL
-FLT
+FLT
T17 /SCTL /11.0E /7.0F
T18
T19
T20
T-BITS
/13.9G /11.0F /10.0E /9.8C /8.5E /7.0B /4.9C /3.5C /2.5H
SLOKL /13.9H
-WPRT
+WPRT
-SKERR
+SKERR
-BSY
+BSY
-RDY
+RDY
T24
T23
T22
T21
-SEL2-3
+SEL2-3
REV. 1.1
DATE :16.6.86
SH 12 OF 14
ISKRA DELTA
DISK CONTROLLER BP+
SMD A-CABLE INTERFACE
CODE NO.


8XK47 H13
8X82R*31 R58
MC3450 K13
8XK47 J13
8X82R*31 R59
MC3450 H13
8XK47 L13
8X82R*31 R60
MC3450 P13
8XK47 N13
8X82R*31 R61
8X10K K12
8XK47 L12
8X82R*31 R62
MC3450 H12
PAL12L10 H12
74F10 E11
74F04 D9
74F74 K10
MC3453 N12
MC3453 P12
BFJ45 T2
BC212*1 T3
BYF405*400 D17
R48 1K0
R68 3K
R70 220R
R67 10R
R69 1K8
CC1 47U
CC3 47N
SLOKH
SLOKL
T-BITS
SMD0L
SMD1L
TAG1L
TAG2L
TAG3L
RDCK
RDATAH
XWCK
PU13
DQUI
WDAT1+
WDAT1-
WDAT3+
WDAT3-
WDAT2+
WDAT2-
WDAT4+
WDAT4-
WCLK1-
WCLK1+
WCLK3-
WCLK3+
WCLK2-
WCLK2+
WCLK4-
WCLK4+
KBC FSOKH
REV. 1.1
DATE 16 6 86
SH 13 OF 14
ISKRA DELTA
DISK CONTROLLER BP+
SMD R/W PORTS INTERFACE
CODE NO.

ST600FR2
J0

1	-TAG1	/12.5F
2	-TAG2	/12.5F
3	-TAG3	/12.5F
4	-BUS0	/12.5B
5	-BUS1	/12.5B
6	-BUS2	/12.5B
7	-BUS3	/12.5C
8	-BUS4	/12.5C
9	-BUS5	/12.5C
10	-BUS6	/12.5C
11	-BUS7	/12.5D
12	-BUSP	/12.5E
13	-BUS9	/12.5E
14	-OPNCBL	/12.5H
15	-FLT	/12.6G
16	-SKERR	/12.6D
17	-ONCYL	/12.6G
18	-IDX	/12.6G
19	-RDY	/12.6D
20		
21	-BSY	/12.6D
22	-USELTAG	/12.5F
23	-SEL0	/12.5G
24	-SEL1	/12.5G
25	-SCT	/12.6G
26	-SEL2-3	/12.6C
27		
28	-WPRT	/12.6D
29	P1CK	/12.3A
30	-BUS10	/12.5E
31	+TAG1	/12.5F
32	+TAG2	/12.5F
33	+TAG3	/12.5F
34	+BUS0	/12.5B
35	+BUS1	/12.5B
36	+BUS2	/12.5B
37	+BUS3	/12.5C
38	+BUS4	/12.5C
39	+BUS5	/12.5C
40	+BUS6	/12.5C
41	+BUS7	/12.5D
42	+BUS8	/12.5E
43	+BUS9	/12.5E
44	+OPNCBL	/12.5H
45	+FLT	/12.6F
46	+SKERR	/12.6D
47	+ONCYL	/12.6G
48	+IDX	/12.6G
49	+RDY	/12.6D
50		
51	+BSY	/12.6D
52	+USELTAG	/12.5F
53	+SEL0	/12.5H
54	+SEL1	/12.5G
55	+SCT	/12.6G
56	+SEL2-3	/12.6B
57		
58	+WPRT	/12.6D
59	HOLD	/12.3A
60	+BUS10	/12.5E

ST260FR2
J1

1		
2	-SCLK1	/13.0G
3	-RDATA1	/13.0H
4		
5	-RDCLK1	/13.0H
6	WCLK1+	/13.9D
7		
8	WDAT1-	/13.7D
9	SEL0+	/13.4H
10	-SKEND1	/13.0G
11		
12		
13		
14	+SCLK1	/13.0G
15		
16	+RDATA1	/13.0G
17	+RDCLK1	/13.0H
18		
19	WCLK1+	/13.9D
20	WDAT1+	/13.7D
21		
22	SEL0-	/13.4H
23	+SKEND1	/13.0G
24		
25		
26		

ST260FR2
J2

1		
2	-SCLK2	/13.0E
3	-RDATA2	/13.0F
4		
5	-RDCLK2	/13.0F
6	WCLK2-	/13.9D
7		
8	WDAT2-	/13.7D
9	SEL1+	/13.4G
10	-SKEND2	/13.0F
11		
12		
13		
14	+SCLK2	/13.0E
15		
16	+RDATA2	/13.0F
17	+RDCLK2	/13.0F
18		
19	WCLK2+	/13.9D
20	WDAT2+	/13.7D
21		
22	SEL1-	/13.4H
23	+SKEND2	/13.0F
24		
25		
26		

ST260FR2
J3

1		
2	-SCLK3	/13.0D
3	-RDATA3	/13.0D
4		
5	-RDCLK3	/13.0D
6	WCLK3-	/13.9D
7		
8	WDAT3-	/13.7D
9	SEL2+	/13.4G
10	-SKEND3	/13.0D
11		
12		
13		
14	+SCLK3	/13.0D
15		
16	+RDATA3	/13.0D
17	+RDCLK3	/13.0D
18		
19	WCLK3+	/13.9D
20	WDAT3+	/13.7D
21		
22	SEL2-	/13.4G
23	+SKEND3	/13.0D
24		
25		
26		

ST260PR2
J4

1		
2	-SCLK4	/13.0B
3	-RDATA4	/13.0B
4		
5	-RDCLK4	/13.0B
6	WCLK4-	/13.9D
7		
8	WDAT4-	/13.7D
9	SEL3+	/13.4G
10	-SKEND4	/13.0B
11		
12		
13		
14	+SCLK4	/13.0B
15		
16	+RDATA4	/13.0B
17	+RDCLK4	/13.0B
18		
19	WCLK4+	/13.9D
20	WDAT4+	/13.7D
21		
22	SEL3-	/13.4G
23	+SKEND4	/13.0B
24		
25		
26		

REV. 1.1	DATE		SH 14 OF 14	
ISKRA DELTA	CONNECTORS			CODE NO.

PREGLED VARIANT V SESTAVNICI

Var.	Ident variante	Naziv
01A	20275044	PODNOŽJE VT.E. DD11-PK - DE

Var.	Ident variante	Naziv

PREGLED IZDAJ IN SPREMEMB V SESTAVNICI

Izd.	Obvestilo	Datum obvestila	Št. sp.	Opis spremembe	Velja za varianto	Datum izdaje	Referent	Avtor izdaje	Po avt
01	12-081	86.12.09		NOVA SESTAVNICA	A / / / / /	9.12.86	03	JEFIČ M.	

Iskra Delta

NASLOVNI LIST SESTAVNICE

PODNOŽJE VT.E. DD11-PK - DE

Obvest. – Nalog	Datum izpisa	Izdaja	Ident sestavnice	Dekada	List
12-081	9.12.86	01	20275044	01A	

N – neaktiven (brez datuma)
– neaktiven (do datuma)

D – kupljeni del (brez strukture)
E – lastni del (s strukturo)
Q – usluge
I – drobni inventar
L – kabli, povezave, žice (odrezane na dolžino)
M – material, ki ga kupujemo

T – orodje,
U – dokumentacija, literatura
V – servisni material (za vzdrževanje)
Z – izdelek, lastni produkt
Q – programska oprema na mediju

P – prototipna razvojna faza
R – proizvodnja rezervnih delov
S – serijska proizvodnja
T – tehnološki sestav, ki se ne skladišči
Z – proizvodna storitev za zunanjega naročnika

3 – lastni produkt ID – izdelan v SOZD po dokumentaciji ID
4 – lastni produkt ID – izdelan izven SOZD po dokumentaciji ID
6 – izdelek v prejanjih cenilih ID
6 – prosto
7 – kupljenec s kliringa – ni naš razvoj

9 – kupljenec domači – ni naš razvoj
0 – prosto

4 – m (meter)
5 – m² (kvadratni meter)
6 – m³ (kubični meter)
7 – g (gram)
8 – ml (mililiter)
9 – par (po dva kosa)
0 – garnitura

3 – za 1000 = 10³ kosov
4 – za 10000 = 10⁴ kosov
5 – za 100000 = 10⁵ kosov
6 – za 1000000 = 10⁶ kosov

Poz.	Ident	Naziv	Napotilo	S	K	P	I	EM	BF	Količina za vnos						Velja
										A						
01A	20275044	PODNOŽJE VT.E. DD11-PK - DE		A	S		2	1	0	*						
001	29841044	PODNOŽJE VT.E. DD11-PK-SK		A	D		8	1	0	1						
002	20285044	NOSILEC VEZ. PLOŠČE-VZDOLŽNI		A	E		6	1	0	2						
003	20286044	NOSILEC VEZ. PLOŠČE-PREČNI		A	E		6	1	0	3						
004	22014044	NOSILEC KONEKTORJA PREČNI	21784044	A	E		6	1	0	2						
005	01100091	VIJAK M3X12 JE4 ZN20KR	IS-F,03,01	A	M		9	1	0	9						
006	17838091	VIJAK M4X12 JE4 ZN20KR	Y-M,B1,111	A	M		9	1	0	14						
007	03534091	VIJAK M3X10 JE3 ZN20KR	IS-F,03,18	A	M		9	1	0	4						
008	05805091	PODLOŽKA 03 JEV ZN20KR	IS-F,06,14	A	M		9	1	0	4						
009	20300044	VODNIK TM70 8R*1,0	TP-L,07,103	A	L		9	4	2	7						
010	29862044	SPOJKA OBESNA SM*3,3/0,5-1		A	M		9	1	0	1						

Iskra Delta	SESTAVNICA	Avtor izdaje	Obvest. – Nalog	Datum izpisa	Izdaja	Ident sestavnice	Dekada	Li
	PODNOŽJE VT.E. DD11-PK - DE	JEFIĆ M.	12-081	9.12.86	01	20275044	01*	

PREGLED VARIANT V SESTAVNICI

Var.	Ident variante	Naziv
01	20279044	PODNOŽJE VT.E, DD11-DK - DE

Var.	Ident variante	Naziv

PREGLED IZDAJ IN SPREMEMB V SESTAVNICI

Izd.	Obvestilo	Datum obvestila	Št. sp.	Opis spremembe	Velja za varianto	Datum izdaje	Referent	Avtor izdaje	Po av
01	12-092	86,12,05		NOVA SESTAVNICA	A / / / / /	9,12,86	03	JEFIČ M,	

Iskra Delta

NASLOVNI LIST SESTAVNICE

PODNOŽJE VT.E, DD11-DK - DE

Obvest. – Nalog	Datum izpisa	Izdaja	Ident sestavnice	Dekada	List
12-092	9,12,86	01	20279044	01	

- neaktiven (brez datuma)
- neaktiven (do datuma)

D – kupljeni del (brez strukture)
E – lastni del (s strukturo)
I – drobni inventar
L – kabli, povezave, žice (odrezane na dolžino)
M – material, ki ga kupujemo
T – orodje
U – dokumentacija, literatura
V – servisni material (za vzdrževanje)
Z – izdelek, lastni produkt
Q – programska oprema na mediju

P – prototipna razvojna faza
R – proizvodnja rezervnih delov
S – serijska proizvodnja
T – tehnološki sestav, ki se ne skladišči
Z – proizvodna storitev za zunanjega naročnika

3 – lastni produkt ID – izdelan v SOZD po dokumentaciji ID
4 – lastni produkt ID – izdelan izven SOZD po dokumentaciji ID
5 – izdelek v prejšnjih cenikih ID
6 – prosto
7 – kupljenec s klicnga – ni naš razvoj
9 – kupljenec domači – ni naš razvoj
0 – prosto

1 – kg (kilogram)
3 – l (liter)
4 – m (meter)
5 – m² (kvadratni meter)
6 – m³ (kubični meter)
7 – g (gram)
8 – ml (mililiter)
9 – par (po dva kosa)
0 – garnitura

1 – za 10 = 10^1 kosov
2 – za 100 = 10^2 kosov
3 – za 1000 = 10^3 kosov
4 – za 10000 = 10^4 kosov
5 – za 100000 = 10^5 kosov
6 – za 1000000 = 10^6 kosov

Poz.	Ident	Naziv	Napotilo	S	K	P	I	EM	BF	Količina za vnos A	Velja d
01A	20279044	PODNOŽJE VT.E. DD11-DK - DE		A	S		2	1	0	*	
001	29840044	PODNOŽJE VT.E. DD11-DK-SK		A	D		8	1	0	1	
002	20285044	NOSILEC VEZ. PLOŠČE-VZDOLŽNI		A	E		6	1	0	2	
003	20286044	NOSILEC VEZ. PLOŠČE-PREČNI		A	E		6	1	0	3	
004	22014044	NOSILEC KONEKTORJA PREČNI	21784044	A	E		6	1	0	2	
005	01100091	VIJAK M3X12 JE4 ZN20KR	IS-F,03,01	A	M		9	1	0	9	
006	17888091	VIJAK M4X12 JE4 ZN20KR	Y-M,B1,111	A	M		9	1	0	14	
007	03536091	VIJAK M3X10 JE5 ZN20KR	IS-F,03,18	A	M		9	1	0	4	
008	05905091	PODLOŽKA A3 JEV ZN20KR	IS-F,06,14	A	M		9	1	0	4	
009	20300044	VODNIK TM70 ØR*1,0	TP-L,07,103	A	L		9	4	2	7	
010	29862044	SPOJKA OKESNA SN*3,3/0,3-1		A	M		9	1	0	1	

Iskra Delta	SESTAVNICA	Avtor izdaje	Obvest. – Nalog	Datum izpisa	Izdaja	Ident sestavnice	Dekada	Lis
	PODNOŽJE VT.E. DD11-DK - DE	JEFIĆ M.	12-082	9.12.86	01	20279044	01*	

PREGLED VARIANT V SESTAVNICI

Var.	Ident variante	Naziv
01*	20277044	PODNOŽJE VT.E. DD11-MK - DE

Var.	Ident variante	Naziv

PREGLED IZDAJ IN SPREMEMB V SESTAVNICI

Izd.	Obvestilo	Datum obvestila	Št. sp.	Opis spremembe	Velja za varianto	Datum izdaje	Referent	Avtor izdaje	Pod avto
01	12-083	84.12.07		NOVA SESTAVNICA	A / / / / /	9.12.84	03	JEFIĆ M.	

Iskra Delta

NASLOVNI LIST SESTAVNICE

PODNOŽJE VT.E. DD11-MK - DE

Obvest. – Nalog	Datum izpisa	Izdaja	Ident sestavnice	Dekada	List
12-083	9.12.84	01	20277044	01*	

A – neaktiven (brez datuma)
– neaktiven (do datuma)

D – kupljeni del (brez strukture)
E – lastni del (s strukturo)
G – usluge
I – drobni inventar
L – kabli, povezave, žice (odrezane na dolžino)
M – material, ki ga kupujemo

T – orodje
U – dokumentacija, literatura
V – servisni material (za vzdrževanje)
Z – izdelek, lastni produkt
Q – programska oprema na mediju

R – proizvodnja rezervnih delov
S – serijska proizvodnja
T – tehnološki sestav, ki se ne skladišči
Z – proizvodna storitev za zunanjega naročnika

3 – lastni produkt ID – izdelan v SOZD po dokumentaciji ID
4 – lastni produkt ID – izdelan izven SOZD po dokumentaciji ID
6 – izdelek v prejšnjih osnovah ID
8 – prosto
7 – kupljenec s kliringa – ni naš razvoj
9 – kupljenec domači – ni naš razvoj
0 – prosto

1 – kg (kilogram)
3 – l (liter)
4 – m (meter)
5 – m² (kvadratni meter)
6 – m³ (kubični meter)
7 – g (gram)
8 – ml (mililiter)
9 – par (za dva kosa)
0 – garnitura

1 – ZA 10 = 10^1 kosov sestavnice
2 – ZA 100 = 10^2 kosov sestavnice
3 – ZA 1000 = 10^3 kosov sestavnice
4 – ZA 10000 = 10^4 kosov sestavnice
5 – ZA 100000 = 10^5 kosov sestavnice
6 – ZA 1000000 = 10^6 kosov sestavnice

Poz.	Ident	Naziv	Napotilo	S	K	P	I	EM	BF	Količina za vnos A	Velja do
01A	20277044	PODNOŽJE VT.E. DD11-MK - DE		A	S		2	1	0	*	
001	26900044	PODNOŽJE DD11-MK-SK		A	D		8	1	0	1	
002	20285044	NOSILEC VEZ. PLOŠČE-VZDOLŽNI		A	E		6	1	0	2	
003	20286044	NOSILEC VEZ. PLOŠČE-PREČNI		A	E		6	1	0	3	
004	22014044	NOSILEC KONEKTORJA PREČNI	21784044	A	E		6	1	0	2	
005	01100091	VIJAK M3X12 JE4 ZN20KR	IS-F.03.01	A	M		9	1	0	9	
006	17888091	VIJAK M4X12 JE4 ZN20KR	Y-M.B1.111	A	M		9	1	0	14	
007	03336091	VIJAK M3X10 JE3 ZN20KR	IS-F.03.18	A	M		9	1	0	4	
008	05805091	PODLOŽKA AS JEV ZN20KR	IS-F.06.14	A	M		9	1	0	4	
009	20300044	VODNIK TM70 ØR*1,0	TP-L.07.103	A	L		9	4	2	7	
010	29862044	SPOJKA DSESNA 3N*0,3/0,3-1		A	M		9	1	0	1	

Iskra Delta	SESTAVNICA	Avtor izdaje	Obvest. – Nalog	Datum izpisa	Izdaja	Ident sestavnice	Dekada	List
	PODNOŽJE VT.E. DD11-MK - DE	JEFIČ M.	12-083	9.12.86	01	20277044	01*	1